Design of Ternary Content-Addressable Memories with Dynamically Power-gated Storage Cells Using FinFETs

Meng-Chou Chang, Kai-Lun He, and Yu-Chieh Wang

***Abstract*—An independent-gate FinFET can operate in two modes: SG (shorted-gate) and IG (independent-gate) modes, and thus a FinFET-based circuit offers rich design options for lower power, better performance or reduced transistor count. In this paper, we present two novel dynamically power-gated FinFET TCAM cells, called DPG-17T and DPG-16T, which power-gate the prefix data storage unit when storing a 'don't care' value. With the dynamic power-gating mechanism, DPG-17T/DPG-16T achieve lower power dissipation by eliminating the switching power of the comparison FinFETs and suppressing the leakage power of the prefix data storage when storing a 'don't care' value. Moreover, the discharge path of the matchline in DPG-17T/DPG-16T can be constructed with only one FinFET instead of two FinFETs, greatly boosting the search speed. Simulation results have shown that a TCAM of 64-word×128-bit using DPG-17T/DPG-16T can reduce the worst-case search delay by 53.0%/53.6% and improve the energy-delay product by 68.5%/70.4% when operating under a search rate of 4.0 GHz.**

***Index Terms*—Ternary content-addressable memories (TCAM), FinFET, power gating, low-power electronics.**

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I. Introduction

FINFET (fin-type field-effect transistor) has emerged as one of the best substitutes for planar MOSFET technology to enable further CMOS scaling. As shown in Fig.1, the FinFET device structure consists of a thin fin-shaped silicon body surrounded by shorted or independent gates on either side of the fin, constructed on SOI (silicon-on-insulator) [1]-[3] or bulk substrates [4], [5]. The FinFET device offers the following advantages [6]: 1) As the fin silicon body is generally thin enough with the thickness of the fin, denoted by T_{si}, smaller than the channel length, denoted by L_g, the gate electrode of the FinFET device has superior control over the channel, thereby suppressing the short-channel effects and leading to reduced subthreshold leakage, steeper subthreshold swing, and a higher I_{on}/I_{off} ratio; 2) As the thin silicon body of the FinFET device is typically undoped or lightly doped, the carrier mobility is thus enhanced with ionized dopant scattering eliminated, and the device variations due to random dopant fluctuation (RDF) are reduced.

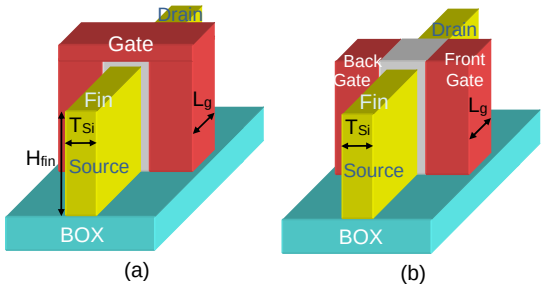

Fig. 1. FinFET device structures. (a) Shorted-gate FinFET. (b) Independent-gate FinFET.

As illustrated in Fig. 1, a FinFET device can be constructed as a shorted-gate FinFET (Fig. 1(a)) or as an independent-gate FinFET (Fig. 1(b)). In the shorted-gate FinFET, the gate controls the channel from both sides and the top of the thin silicon body, leading to increased process transconductance. In the independent-gate FinFET, the top part of the gate is etched away, resulting in two independent gates, the front gate and the back gate. The front gate and back gate of an independent-gate FinFET can be separately controlled by two independent signals, and thus an independent-gate FinFET can be used as a pair of parallel planar MOSFETs controlled by two independent signals.

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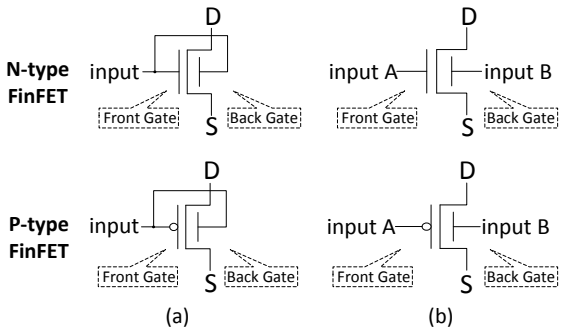

Fig 2. Two operating modes of a FinFET. (a) Shorted-gate (SG) mode. (b) Independent-gate (IG) mode.

As illustrated in Fig. 2, a FinFET can operate in two modes: shorted-gate (SG) and independent-gate (IG) modes. In the SG mode, the front gate and the back gate of the FinFET are tied together and controlled by a single input signal (see Fig. 2(a)). A SG-mode FinFET has the advantage of providing the maximum drive strength when it is turned on. In the IG mode (see Fig. 2(b)), the front gate and the back gate of the FinFET are separately controlled. An IG-mode FinFET can be employed to replace a pair of parallel planar MOSFETs. As a FinFET device can operates in two modes: SG and IG modes, a FinFET-based circuit offers rich design options for lower power dissipation or reduced transistor count. Many innovative FinFET-based circuit styles have been proposed in the literature [7]-[13]. In [7], a single independent-gate FinFET is used to replace a pair of parallel transistors in the pull-up or pull-down networks of logic gates to obtain a compact low-power implementation of the same Boolean function. In [8], the authors explored the performance and power characteristics of FinFET-based NAND gates configured in various modes, including the SG, IG, LP (low-power) modes and a hybrid IG/LP mode. In [9], the authors investigated the design space of elementary logic gates, latches, and flip-flops in FinFET technology for optimal tradeoffs in leakage versus delay. In [10], the authors explored the possibility of using a single dual-V_{th} independent-gate FinFET to replace series transistors in the pull-up or pull-down networks of logic gates. Particularly, many published works are devoted to the design of FinFET-based SRAM cells [11]-[13].

A content-addressable memory (CAM) is a special type of memory that compares the input search word with all data words stored in the memory simultaneously and then returns the address of the matching data word. CAMs facilitate high-speed lookup operation and have been employed in numerous applications, such as data compression [14], image coding [15], Hough transform [16], and associative caches [17]. CAM is classified into two types: binary CAM (BCAM) and ternary CAM (TCAM). A BCAM cell stores either a logic '0' or a logic '1' while a TCAM cell can store an additional state, '*don't care*' (denoted by 'x'), for supporting wildcard matching. Owing to this partial-match feature, TCAMs can be used to implement the routing tables in network routers for accelerating IP packet classification and forwarding [18]. However, CAMs consume substantial dynamic and static power due to their parallel search operation and large memory array. Various low-power techniques have been developed to reduce the dynamic power dissipation of CAMs [19]-[22]. These techniques include low-swing schemes [19], current-racing schemes [20], current-saving schemes [21], pipelining schemes [22], and so on. Particularly, in [23], the dynamic power source (DPS) scheme was proposed to suppress the leakage power dissipation of TCAM. The key idea behind the DPS scheme is that the prefix storage unit in an asymmetric TCAM cell with 'x' state can be power-gated to suppress leakage dissipation since the prefix data associated with an 'x' bit is useless for determining the match result.

In this paper, we propose two novel dynamically power-gated FinFET TCAM cells, called DPG-17T and DPG-16T, which power-gate the prefix data storage unit when storing a 'don't care' value. With the dynamic power-gating mechanism, DPG-17T/DPG-16T can achieve lower power dissipation by eliminating the switching power of the comparison FinFETs and suppressing the leakage power of the prefix data storage when storing a 'don't care' value.

The remainder of this paper is organized as follows. In Section II, we present the operation of the asymmetric TCAM cell and introduce a FinFET TCAM cell, called Base-16T, which is used as a basis for comparison with the proposed dynamically power-gated FinFET TCAM cells. In Section III, we present the proposed dynamically power-gated FinFET TCAM cells, DPG-17T and DPG-16T. Section IV presents the simulation results which are obtained from HSPICE simulations using the PTM (Predictive Technology Model) 32-nm FinFET models [24]. Section V concludes this paper.

II. BACKGROUND

A. Traditional Asymmetric TCAM Cells

Fig. 3 shows the block diagram of a typical TCAM, consisting of an array of TCAM cells, a search data register, and a column of sense amplifiers.

Each row of the TCAM cell array stores one data word

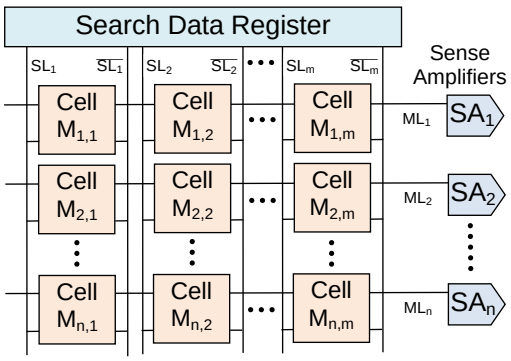

Fig. 3. Block diagram of a typical TCAM with a size of *n*-word×*m*-bit.

together with the associated mask word, and has one associ ated matchline (ML), which is used to indicate whether the stored data word on this row matches or mismatches the search data word. Each column of the TCAM cell array has a

pair of searchlines, SL and $\overline{SL}$, which are used to broadcast the associated search data bit and its complement to all TCAM cells in this column.

Before the search operation begins, all matchlines are precharged to HIGH, and all searchlines are discharged to LOW. The search operation begins by loading the search data word into the search data register and enabling the searchline drivers to broadcast the search data word to the TCAM cell array via searchlines. Then, each TCAM cell compares its stored data bit with the search bit on the corresponding searchlines, and the result of comparison, match or mismatch, affects whether the associated matchline should be discharged.

In a NOR-matchline TCAM, all the TCAM cells belonging to the same row are connected in parallel, and any single-bit mismatch on this row will create a conducting path from the associated matchline to ground, causing the associated matchline to discharge. That is, in a NOR-matchline TCAM, after the search process, a matchline remaining precharged indicates a match condition (i.e., the associated stored data word matches the search data word), and a discharged matchline indicates a mismatch condition (i.e., the associated stored data word mismatches the search data word).

A TCAM cell provides two basic functions: bit storage and bit comparison. The structure of the asymmetric TCAM cell is shown in Fig. 4. An asymmetric TCAM cell consists of four subunits: the prefix data storage, the mask storage, the XOR unit, and the matchline control unit.

The prefix data storage stores the associated data bit, D, together with its complement, $\overline{D}$; the mask storage stores the

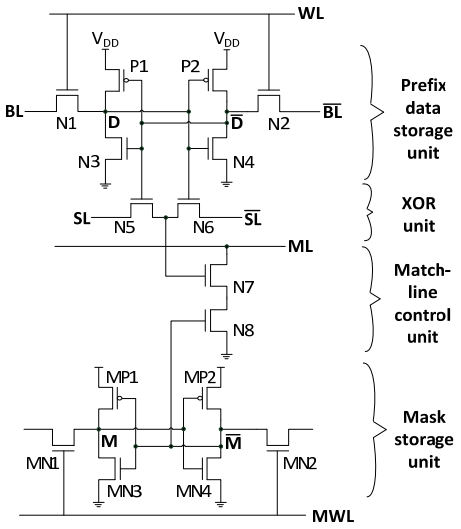

Fig. 4. The structure of the asymmetric TCAM cell.

associated mask bit, M, together with its complement, $\overline{M}$. A TCAM cell can store a ternary value ('0', '1', and 'x'): if the TCAM cell stores a logic '1', D=1 and M=0; if the TCAM cell stores a logic '0', D=0 and M=0; if the TCAM cell stores an 'x', M=1 and D can be either 0 or 1.

The XOR unit is used to compare the stored data bit, D/$\overline{D}$, with the associated search data bit, SL/$\overline{SL}$, on the searchline. If the stored data bit mismatches the search data bit, the gate of NMOS N7 is set to HIGH, and thus N7 is turned on; otherwise, the gate of NMOS N7 is set to LOW, and N7 is turned off.

The matchline-control unit, comprised of transistors N7 and N8, controls whether the precharged matchline (ML) should be discharged. If the mask bit M/$\overline{M}$ is 0/1 (i.e., the stored data bit is not an 'x'), transistor N8 is turned on, and the matchline-control unit creates a conducting pull-down path from the matchline ML to ground if N7 is also turned on (i.e., the stored data bit mismatches the search data bit). On the contrary, if the mask bit M/$\overline{M}$ is 1/0 (i.e., the stored data bit is an 'x'), transistor N8 is turned off, cutting off the discharge path (comprised of N7 and N8) from the matchline, which is consistent with the fact that a stored 'x' bit always matches the search data bit no matter whether the search data bit is 0 or 1.

B. The Base FinFET TCAM cell

As stated earlier, a FinFET can operate in two modes: SG and IG modes (Fig. 2). In the SG mode, the front gate and the back gate of the FinFET are tied together and controlled by a single input signal. A SG-mode FinFET has the advantage of providing the maximum drive strength when it is turned on. In the IG mode, the front gate and the back gate of the FinFET are separately controlled. Thus, an IG-mode FinFET can be employed to replace a pair of parallel planar MOSFETs.

In our previous work [25], we have explored the optimal configuration for the asymmetric FinFET-based TCAM cell. By varying the operating mode (SG/IG) for every FinFET in the TCAM cell, and measuring the resultant performance for various combinations of operating modes, we have acquired the best FinFET TCAM cell configuration, called Base-16T and depicted in Fig. 5(a), in terms of minimum energy-delay product. In Base-16T, FinFETs N5 and N6 are assigned SG mode to accelerate the XOR operation; FinFETs N7 and N8 are also assigned SG mode because they are on the matchline discharge path and play a critical role in determining the worst-case search delay of the TCAM; the other FinFETs, which are not critical in determining the worst-case search delay, are assigned the IG mode to reduce the leakage powerdissipation of the TCAM.

In the following sections, Base-16T will be used as the base FinFET TCAM cell for performance comparison with the proposed dynamically power-gated FinFET TCAM cells.

III. Dynamically Power-gated FinFET TCAM Cells

A TCAM cell can store a ternary value: '0', '1', or 'x'. If an asymmetric TCAM cell stores an 'x' (i.e., M/$\overline{M}$=1/0), the stored data bit, D/$\overline{D}$, is meaningless and useless for determining the final match result during a search operation. Hence, the prefix data storage unit in a TCAM cell storing an 'x' can be dynamically power-gated to suppress the power dissipation of the TCAM cell without impeding the normal search operation of the TCAM. In this work, we propose two novel dynamically power-gated FinFET TCAM cells, called DPG-17T (Fig. 6(a)) and DPG-16T (Fig. 7(a)), which power-gate the prefix data storage unit when storing an 'x' in order to suppress the leakage power dissipation of the TCAM.

In order to assess and compare the performance of three types of FinFET TCAM cells - including Base-16T, DPG-17T, and DPG-16T - we have implemented a NOR-matchline TCAM with a size of 64-word×128-bit for each type of FinFET TCAM

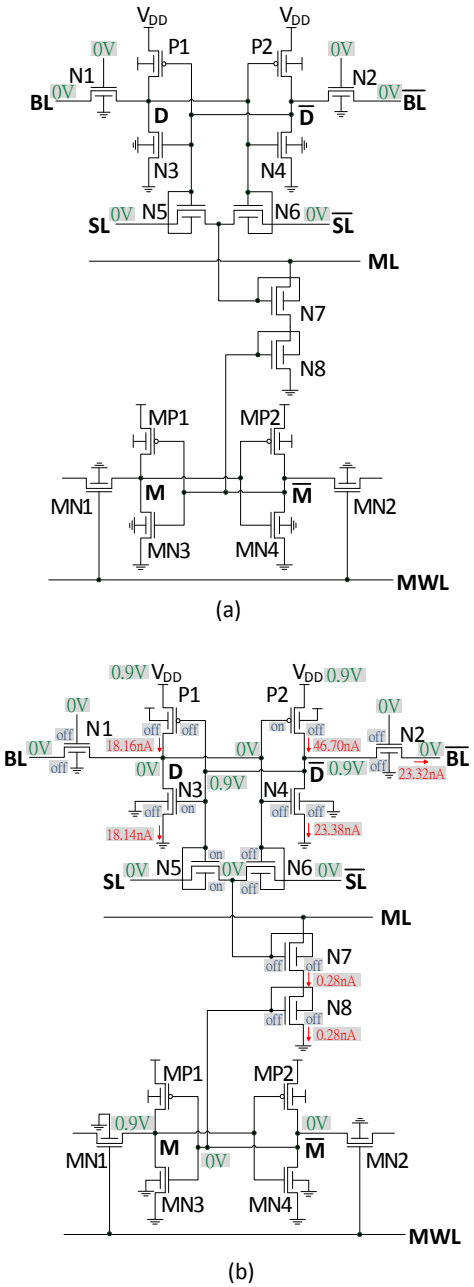

Fig 5. (a) The base FinFET TCAM cell – Base-16T. (b) Base-16T with node voltages and I_{sub} labeled for D = 0, M = 1 and SL/$\overline{SL}$ =0/0.

cells, and have performed the associated HSPICE simulations using the PTM (Predictive Technology Model) 32-nm FinFET models [24] at the typical PVT case (i.e., TT process corner, 25 °C, V_{DD} = 0.9 V). In our simulations, all FinFETs in the TCAM cells are sized minimum with fin height H_{fin} = 32 nm, fin thickness T_{si} = 16 nm, and channel length L_g = 32 nm. Table I shows the subthreshold leakage current (I_{sub}) and the leakage power (P_{leak}) for each FinFET in the three types of FinFET

TABLE I. SUBTHRESHOLD LEAKAGE CURRENT (I_{SUB}) AND LEAKAGE POWER (P_{LEAK}) FOR EACH FINFET IN THREE TYPES OF FINFET TCAM CELLS.

	Base FinFET TCAM cell Base-16T		FinFET TCAM cell DPG-17T		FinFET TCAM cell DPG-16T	
FinFET	I_{sub} (nA)	P_{leak} (nW)	I_{sub} (nA)	P_{leak} (nW)	I_{sub} (nA)	P_{leak} (nW)
P1	18.16	16.35	6.67	1.10	0.00	0.00
P2	46.70	0.00	6.67	1.10	0.00	0.00
P3	-	-	13.34	9.81	-	-
N1	0.00	0.00	0.00	0.00	0.00	0.00
N2	23.32	20.99	0.00	0.00	0.00	0.00
N3	18.14	0.00	6.67	0.00	0.00	0.00
N4	23.38	21.04	6.67	0.00	0.00	0.00
N5	0.00	0.00	0.00	0.00	0.00	0.00
N6	0.00	0.00	0.00	0.00	0.00	0.00
N7	0.28	0.01	0.66	0.02	0.66	0.02
N8	0.28	0.00	0.00	0.00	0.00	0.00
MP1	46.70	0.00	46.70	0.00	46.72	0.00
MP2	18.15	16.34	18.15	16.34	18.15	16.34
MN1	23.32	20.99	23.32	20.99	23.32	20.99
MN2	0.00	0.00	0.00	0.00	0.00	0.00
MN3	23.39	21.05	23.39	21.05	23.39	21.05
MN4	18.14	0.00	18.14	0.00	18.14	0.00
Total P_{leak}	-	116.76	-	70.41	-	58.40

TCAM cells when the TCAM cell stores an 'x' and is idle (i.e., not in the process of a search operation).

Let us first consider Base-16T (see Fig. 5(b)) and assume that the stored data bit D/$\overline{D}$ is 0/1 (i.e., the voltage level of node D/$\overline{D}$ is 0 V/0.9 V) and the TCAM is not performing a search operation (i.e., the TCAM is idle and SL/$\overline{SL}$ is 0 V/0 V). As given in Table I and Fig. 5(b), even though FinFETs P1, N2, and N4 in Base-16T are turned off, there still exist significant subthreshold leakage currents flowing through those FinFETs due to a large voltage drop of 0.9 V across the drain and source of those FinFETs (i.e., P1, N2, and N4). From Table I, Base-16T has a static power dissipation of 116.76 nW when storing an 'x' and being idle.

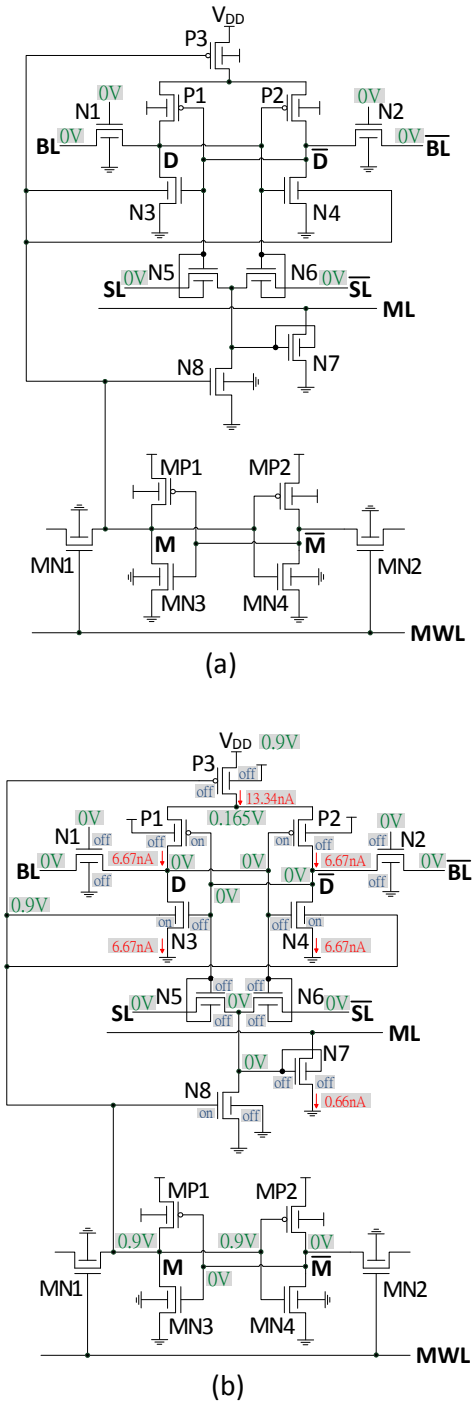

Fig 6. (a) The proposed dynamically power-gated FinFET TCAM cell DPG-17T. (b) DPG-17T with node voltages and I_{sub} labeled for M = 1 and SL/$\overline{SL}$ =0/0.

The first proposed dynamically power-gated FinFET TCAM cell DPG-17T is shown in Fig. 6 (a). The differences between DPG-17T and Base-16T include: 1) DPG-17T has an additional sleep FinFET P3, 2) the operating mode of both N3 and N4 in DPG-17T is changed from SG mode to IG mode with the back gates of both N3 and N4 connected to the mask data bit (node M), and 3) the discharge path of the matchline in DPG-17T is comprised of only one FinFET N7 instead of two FinFETs, leading to a much smaller worst-case search delay. Noted that FinFET N8 is not located on the discharge path of the matchline, and its purpose is just to set the gate voltage of N7 to 0 V when the TCAM cell stores an 'x'.

Let us consider DPG-17T (see Fig. 6(b)) and assume that DPG-17T stores an 'x' (i.e., the voltage level of node M/$\overline{M}$ is 0.9 V/0 V) and the TCAM is not performing a search operation (i.e., the TCAM is idle and SL/$\overline{SL}$ is 0 V/0 V). As given in Fig. 6(b), P3 is turned off, causing the voltage level of the drain of P3 to converge to 0.165 V, and the back gates of both N3 and N4 are turned on, causing the voltage level of nodes D and $\overline{D}$ to become 0 V. As given in Table I, compared with the case of Base-16T, the subthreshold leakage currents flowing through P1, N2, and N4 in DPG-17T are greatly reduced because the voltage drop across those FinFETs is very small (see Fig. 6(b)). Overall, a TCAM cell using DPG-17T instead of Base-16T can reduce the leakage power dissipation by 40% when storing an 'x'.

Note that a DPG-17T TCAM cell storing an ‘x’ does not impede the normal search operation of the TCAM. Suppose that the TCAM wants to perform a search operation now. The search data register begins to drive values on the searchlines, and SL/$\overline{SL}$ in Fig. 6(b) will become either 0.9 V/ 0V (if the associated search data bit is ‘1’) or 0 V/0.9 V (if the associated search data bit is ‘0’). In either case, FinFETs N5, N6, and N7 in Fig. 6(b) stay turned off, and thus the TCAM cell storing an ‘x’ will not create a discharge path for the associated matchline. That is, whether the associated matchline will eventually discharge is determined by other TCAM cells with M = 0.

The second proposed dynamically power-gated FinFET TCAM cell DPG-16T is shown in Fig. 7 (a).

In contrast to DGP-17T, which needs an additional sleep FinFET P3 to fulfill power gating, DPG-16T needs no sleep FinFET and accomplishes power gating by connecting node $\overline{M}$ directly to the sources of both FinFETs P1 and P2.

Let us consider DPG-16T (see Fig. 7(b)) and assume that DPG-16T stores an 'x' (i.e., the voltage level of node M/$\overline{M}$ is 0.9 V/0 V) and the TCAM is not performing a search operation (i.e., the TCAM is idle and SL/$\overline{SL}$ is 0 V/0 V). As given in Fig. 7(b), the sources of both FinFETs P1 and P2 are connected to 0 V, and the back gates of both N3 and N4 are turned on, causing the voltage level of nodes D and $\overline{D}$ to become 0 V. As given in Table I, the subthreshold leakage currents flowing through P1, P2, N1, N2, N3, N4, N5, N6, and N8 in DPG-16T all become 0. Overall, a TCAM cell using DPG-16T instead of Base-16T can reduce the leakage power dissipation by 50% when storing an 'x'.

As in the case of DPG-17T, a DPG-16T TCAM cell storing an ‘x’ does not impede the normal search operation of the TCAM.

IV. Simulation Results

Table II gives static power consumption comparison of a TCAM of 64-word×128-bit implemented with three types FinFET TCAM cells - including Base-16T, DPG-17T, and DPG-16T. As the percentage of 'x' bits in the TCAM cell array

has an influence on TCAM power consumption, during our HSPICE simulation, we have set the prefix length distributions of the TCAM simulated close to those of 'AS2.0 IPv6 BGP (Border Gateway Protocol) table data' given in [26]. Since

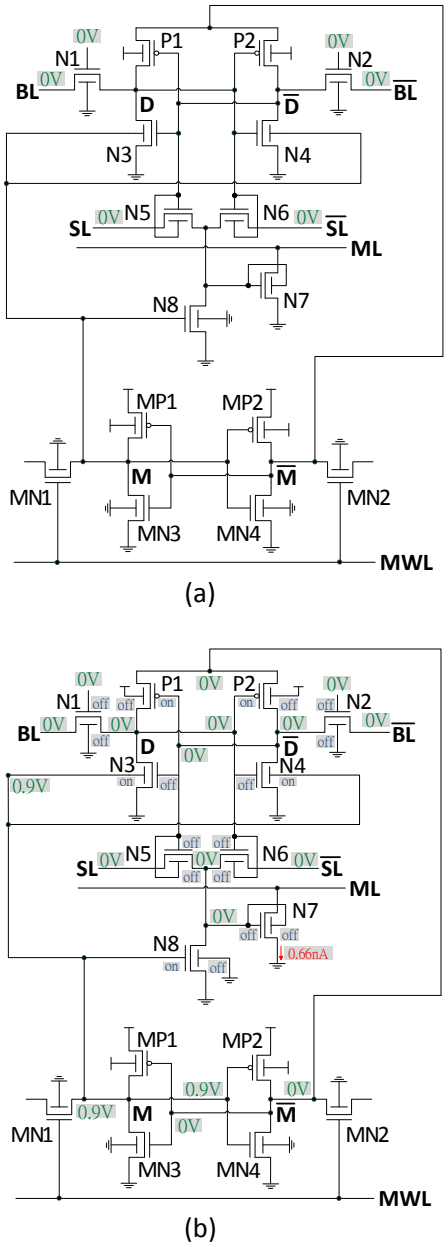

Fig 7. (a) The proposed dynamically power-gated FinFET TCAM cell DPG-16T. (b) DPG-16T with node voltages and I_{sub} labeled for M = 1 and SL/$\overline{SL}$ =0/0.

68.5% of the prefix data bits in the AS2.0 IPv6 BGP table are 'x', the same percentage (i.e., 68.5%) of the prefix data bits in the TCAM simulated are set as 'x'. From Table II, a TCAM employing DPG-17T/DPG-16T, instead of Base-16T, can reduce the static power dissipation by 27.2%/34.2%.

TABLE II. STATIC POWER CONSUMPTION COMPARISON OF A TCAM OF 64-WORD×128-BIT IMPLEMENTED WITH THREE TYPES OF FINFET TCAM CELLS.

	Type of the FinFET TCAM cells used in the TCAM		
	Base-16T	DPG-17T	DPG-16T
Static power consumption of the whole TCAM (μW)	961.3	700.2	632.9

Table III gives performance comparison of three FinFET TCAM cells - including Base-16T, DPG-17T, and DPG-16T - used to implement a TCAM of 64-word×128-bit operating at a search rate of 4.0 GHz. As given in Table III, the use of DPG-17T/DPG-16T, instead of Base-16T, can reduce the TCAM power dissipation by 32.9%/36.3%. The lower power dissipation of DPG-17T/DPG-16T comes from 1) A TCAM cell storing an 'x' always turns off FinFETs N5 and N6, eliminating the switching power of N5 and N6 during comparison, and 2) The prefix data storage unit of a TCAM cell storing an 'x' is power-gated during the search process, consuming only little leakage power. Moreover, since the discharge path of the matchline in DPG-17T/DPG-16T is comprised of only one FinFET rather than two FinFETs as in Base-16T, the worst-case search delay of a TCAM employing DPG-17T/DPG-16T can be greatly reduced. As given in Table III, the use of DPG-17T/DPG-16T, instead of Base-16T, can reduce the worst-case search delay by 53.0%/53.6%, and improve the energy-delay product by 68.5%/70.4%.

TABLE III. PERFORMANCE COMPARISON OF THREE FINFET TCAM CELLS USED TO IMPLEMENT A TCAM OF 64-WORD×128-BIT OPERATING AT A SEARCH RATE OF 4.0 GHZ

	Type of the FinFET TCAM cells used in the TCAM		
	Base-16T	DPG-17T	DPG-16T
Average power for whole TCAM (mW) [**A**]	2.95	1.98	1.88
Worst-case search delay (ps) [**B**]	71.25	33.48	33.07
Search energy for whole TCAM (fJ) [**C**=A·0.25ns]	736.90	495.15	469.73
Search energy per bit (aJ) [**D**=C/64/128]	89.95	60.44	57.34
Energy-delay product (10^{-27}J·s) [**E**=B·D]	6.41	2.02	1.90

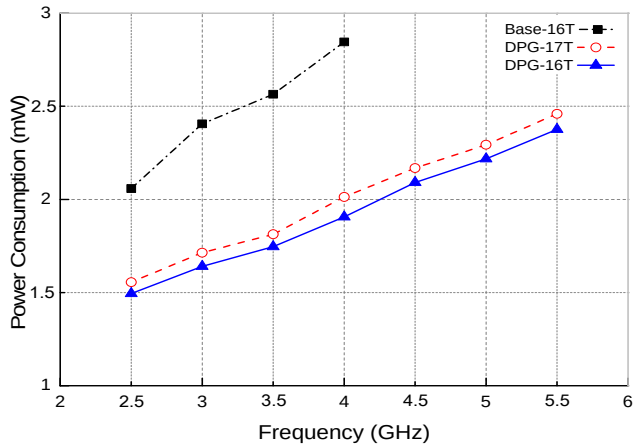

Fig 8. Power consumption comparison of a TCAM of 64-word×128-bit implemented with three types of FinFET TCAM cells.

Fig. 8 gives power consumption comparison of a TCAM of 64-word×128-bit implemented with three types of FinFET TCAM cells, for various search rates. The maximun search rate for the TCAM implemented with Base-16T/DPG-17T/DPG-16T is 4.0/5.5/5.5 GHz. Note that a TCAM with DPG-17T/DPG-16T operating at a higher frequency of 5.5 GHz even consumes less power than a TCAM with Base-16T operating at a lower frequency of 3.5 GHz.

V. Conclusion

In this paper, we have proposed two dynamically power-gated FinFET TCAM cells, DPG-17T and DPG-16T. When operating under a search rate of 4.0 GHz, a TCAM of 64-word×128-bit using DPG-17T/DPG-16T instead of Base-16T can 1) reduce the power dissipation by 32.9%/36.3%, 2) reduce the worst-case search delay by 53.0%/53.6%, and 3) improve the energy-delay product by 68.5%/70.4%.

The advantages of the dynamically power-gated TCAM cells, DPG-17T and DPG-16T, are summarized as follows: 1) The discharge path of the matchline in DPG-17T/DPG-16T is comprised of only one FinFET instead of two, greatly reducing the worst-case search delay, 2) A TCAM cell storing an 'x' always turns off FinFETs N5 and N6, eliminating the switching power of N5 and N6 during comparison, and 3) The prefix data storage unit of a TCAM cell storing an 'x' is power-gated during the search process, suppressing leakage power dissipation.

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