Operational Transconductance Amplifier in 350nm CMOS technology

Dejan D. Mirković, Predrag M. Petković, Ilija Dimitrijević and Igor Mirčić

***Abstract*—This paper presents transistor level design of operational transconductance amplifier in CMOS technology. Custom designed, circuit is to be built-in into the mixed-signal, switched capacitor circuit. Amplifier targets relatively high slew-rate and moderate open loop gain with megahertz order gain-bandwidth. Adopted architecture is discussed appreciating application in switched capacitor circuits. Circuit behavior is examined through set of simulations. Obtained results confirmed desired behavior. Target technology process is TSMC 350nm.**

***Index Terms*—Integrated circuit, Amplifier, Switched capacitor circuits, CMOS technology**

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I. Introduction

OPERATIONAL amplifiers (OA) are considered to be the fundamental parts of analog electronics. Moreover, it is one of the very first circuits with successful tape-out designed in LEDA laboratory in early nineties [1], [2]. OAs appears as inevitable part for analog signal conditioning. Switched capacitor (SC) circuits are not exception. Design covered in this work is meant to be embedded into analog part of the second order ΔΣ analog-to-digital converter (ADC) discussed in [3]. Being part of SC circuits the OA requires relatively high slew-rate and gain-bandwidth. As shown in [4], open loop i.e. DC gain has the smallest influence, comparing to slew-rate and gain bandwidth, on SC circuit characteristics. Therefore moderate open loop gain is sufficient. Because all circuitry will be on-chip, Operational Transconductance Amplifier (OTA) is required. Table I summarizes main OTA design parameters set by the higher order circuit requirements.

Parameters like, input/output dynamic range (DR), common mode (CMRR) and power supply (PSRR) rejection ratios should be as large as possible.

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D. D. Mirković is with the Faculty of Electronic Engineering, University of Niš, Niš, Serbia (phone: +381-18-529-321; fax: +381-18-588-399; e-mail: dejan.mirkovic@elfak.ni.ac.rs).

P. M. Petković is with the Faculty of Electronic Engineering, University of Niš, Niš, Serbia (e-mail: predrag.petkovic@elfak.ni.ac.rs).

I. Dimitrijevič and I. Miričć are the undergraduate students at Faculty of Electronic Engineering, University of Niš, Niš, Serbia.

TABLE I
TARGET OTA PARAMETERS

Parameter	Description	Value
A_0	DC, open loop, gain	> 50 dB
f_{gbw}	Gain-bandwidth	> 120 MHz
SLR	Slew rate	> 120 V/μs

Since TSMC 350nm technology process supports relatively high, 3.3V, power supply voltage DR requirements are expected to be fulfilled.

Circuit supposed to be fully differential which implies utilizing some form of common-mode feedback (CMFB) circuitry. Besides, OTA has to have its own bias point generator in order to provide appropriate transistor operation. Since on-chip capacitors are considered, 2pF differential load capacitance is adopted. This value is also set by higher order circuit requirements concerning kT/C noise of ΔΣ structure explained in [4]. It should be mentioned that target technology process offers Poly-insulator-Poly (PiP) capacitors with 864 aF/μm^2 capacitance per unit area. Hence the value of 2 pF for load capacitance gives reasonably high capacitor area of 2314.81 μm^2 (48.11μm x 48.11μm).

Paper is organized as follows. In second section adopted OTA architecture will be briefly discussed and appropriate subsections will cover circuitry in more details. Third section presents simulation results. Finally, in the fourth section, educative conclusions are drawn and possible improvements are discussed.

II. OTA Architecture

The first step in structural design was to define circuit's architecture. It is well known that cascoding technique is quite often used when high DC gain and PSSR are required without scarifying circuit's dynamics [5]. Although folded cascode (FC) architecture is commonly adopted for building SC circuits; telescopic architecture is chosen for OTA design in this case. Some related work supporting this idea is published in [6], [7]. It is well known that FC provides wider input common-mode range, better input-output common mode relation and high input/output swing [8]. All those advantages imply higher power consumption; lower gain; higher noise and, most importantly in this case, lower speed (i.e. slew-rate and gain-bandwidth). Choosing telescopic architecture means

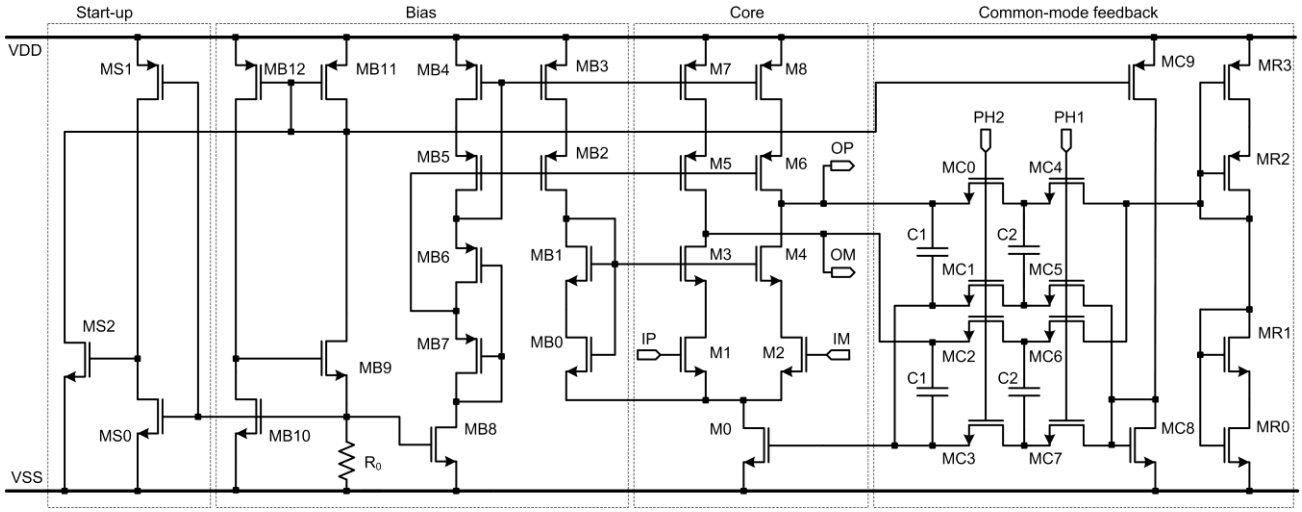

Fig. 1. Telescopic OTA with bias and SC CMFB circuitry.

TABLE II
TRANSISTOR DIMENSIONS

Transistors	width/length [μm/μm]
(M1, M2, M3, M4), (M0, M5, M6, M7, M8)	(128/0.8), (256/0.8)
(MB1, MB8), (MB2, MB3, MB4, MB5, MB7, MB10, MB9),(MB11, MB12), MB0,MB6, MS0, (MS1, MS2)	(128/0.8), (256/0.8), (512/0.8), 24/0.8, 88/0.8, 400/0.8, (4/0.8)
(MC0, MC1, MC2, MC3, MC4, MC5, MC6, MC7, MC8), MC9	(1.6/0.8), 3.2/0.8
(MR1, MR3), MR2, MR0	(2.4/0.8), 7.2/0.8, 0.8/0.8

stricter constraint on input/output common-mode voltage choice. Transistor level schematic of OTA with bias and CMFB circuitry is depicted in Fig. 1. Dimensions of all transistors are summarized in Table II. Design can be partitioned in three sub-blocks namely: Core, Bias with start-up and CMFB.

A. Core

Transistors M0-M8 are the core of the design. Analyzing structure utilizing small-signal model open loop gain is:

$$A_0 \approx g_{m1,2}\left(g_{m3,4}r_{03,4}r_{01,2} \parallel g_{m5,6}r_{05,6}r_{07,8}\right) \quad (1)$$

Cascode configuration by itself provides large DC gain and (1) is expected to meet the DC gain requirements. Being single stage, there is no need for frequency compensation. Stability is also guaranteed by relatively large, 2pF differential load capacitance, C_L. Therefore gain-bandwidth is mainly determined by transconducatance of amplifying devices, $g_{m1,2}$, and load capacitance ratio. Design procedure is as follows. Transconductance of M1 and M2 devices should satisfy the following equation:

$$g_{m1,2} = 2\pi f_{gbw} C_L . \quad (2)$$

For given gain-bandwidth and load capacitance, g_m equals to about 1.5mS. Taking into account fully differential case this value is doubled. In order to properly size amplifying devices set of simulations at room temperature were done. Diagrams shown in Fig. 2, 3 and 4 present obtained results. All those curves are extracted using SPICE [9].

Fig. 2 is created by simulating diode connected device.

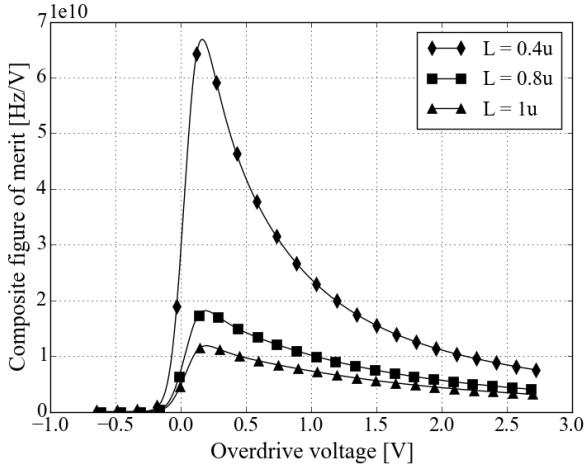

Fig. 2. Composite figure of merit versus overdrive voltage.

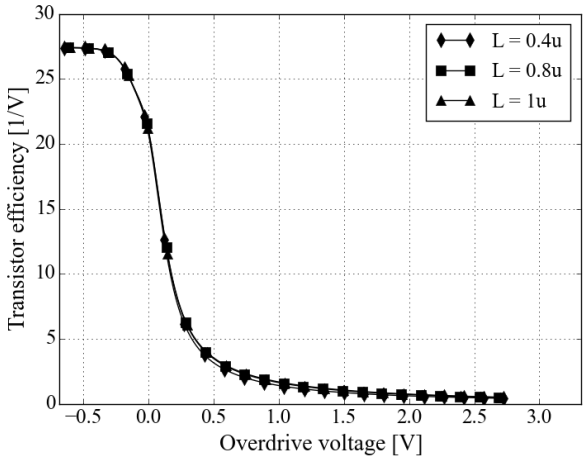

Fig. 3. Transistor efficiency versus overdrive voltage.

It shows composite figure of merit defined as $f_t \times (g_m/I_D)$ versus overdrive voltage, $V_{ov}=V_{GS} - V_{TH}$, where, f_t, is unity current gain frequency and g_m/I_D transistor efficiency. Observing Fig. 2 and Fig. 3 for different channel lengths one can find optimal V_{ov} bias point which compromises between

speed i.e. maximal transistors's operating frequency and efficiency. This value is about 200mV.

Knowing this, the channel current can be extracted. Namely, for overdrive voltage of 200mV Fig. 3 indicates the efficiency of about $10V^{-1}$ which gives the channel current I_D= 300μA.

To pick suitable channel length one should observe Fig. 4 which shows small signal gain, a_{v0}, versus drain-source voltage of the MOS device in target technology for different channel lengths. It is notable that shorter channel lengths give relatively constant a_{v0} in wide dynamic range. On the other hand a_{v0} reduces significantly as length decrees. It is obvious that there is a tradeoff between dynamic range and gain.

If (1) is heavily approximated assuming equal transconductances/resistances, A_0 reduces to $(g_m r_0)^2 = a_{v0}^2$. Picking the L= 0.4μm gives a_{v0} not lower than 20 times in reasonably high dynamic range i.e. 1-3V. Therefore the total gain would be $A_0 \approx 400$ or roughly 52dB. After this value is adopted as good enough the following should be appreciated. Firstly, (1) is heavily approximated and secondly short channel effect is always present. Therefore to mitigate short channel effects, and to ensure gain higher than 50dBs, L= 0.8μm is adopted.

It is also estimated, again using SPICE, that there is a 3.75 μA drain current per 1μm of channel width for chosen transistor efficiency (10) and channel length (0.8μm) in the target technology. Drain current per unit of channel width, I_D/W, versus transistor efficiency is depicted in Fig. 5. Accordingly, for 300μA current the minimal width of amplifying devices is W= 80 μm resulting with width-length ratio of 100. This value sets the initial dimensions and the dimensions of all other transistors are drawn based on it. Eventually, final dimensions end up being larger in order to fully meet requirements given in Table I.

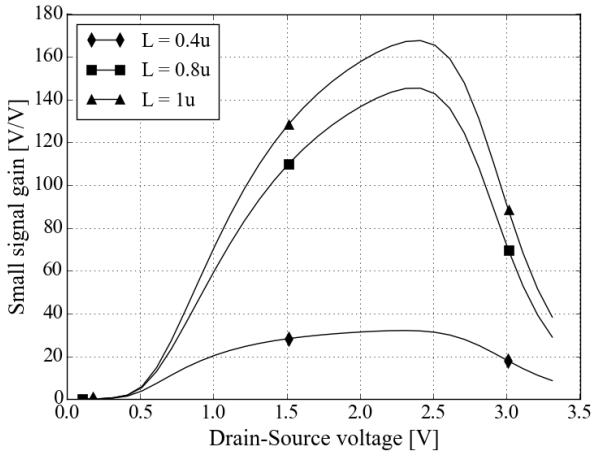

Fig. 4. Small signal gain versus drain-source voltage.

It should be emphasized that these curves are exclusively used to build intuition of how device behaves in various biasing conditions. In other words they serve as guidelines for setting initial design values. Therefore, the designer has the freedom to chose a set of curves which best matches his/hers problem and/or intuition. In this work the most useful ones are covered.

B. Bias with Start-up

Bias circuit is composed of transistors denoted as MB0-MB12 in Fig. 1. Reference current is generated using independent, self biased, V_{TH} reference. This reference uses the fact that sensitivity of the active device voltage to the power supply change is always less than unity. This is governed by square root relation between transistors overdrive voltage and drain current.

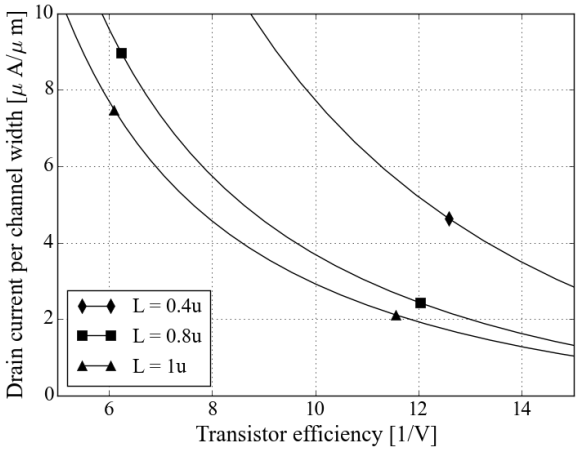

Fig. 5. Drain current per channel width versus transistor's efficiency.

When the circuit is arranged to generate current through an active device according to the overdrive voltage controlled with the same current, result is reference which is for all practical purposes independent of V_{DD}. In this case it is done with transistors MB9-MB12 and resistor, R_0. Practically the gate-source voltage of MB10 equals to voltage drop across R_0 produced by the current trough MB9. Simultaneously it defines drain current value of MB10 which is mirrored back into drain current of MB9 thorough MB11/12 current mirror. This loop provides sustainable reference mainly dependent on R_0 resistance.

From one side current, I_0, in MB9/11 branch is limited by resistor R_0. On the other hand the very same current sets overdrive voltage of MB10. Therefore, equation (3) holds. All values in (3) are referred to transistor MB10.

$$I_0 R_0 = V_{TH} + \sqrt{\frac{2I_0}{\mu_0 C'_{ox}(W/L)}} \tag{3}$$

where μ_0 stands for mobility and C'_{ox} denotes gate oxide capacitance pre unity area. Expressing R_0 from (3), and appreciating relation $g_m^2 = 2\,\mu_0\,C'_{ox}\,(W/L)\,I_0$ (4) arises.

$$R_0 = \frac{V_{TH}}{I_0} + \frac{2}{g_m} \tag{4}$$

Choosing I_0= 600μA (tail source M0), g_m = 6mS (assuming relatively constant overdrive voltage of M0/MB10) and

knowing that V_{TH} for NMOS device in the target technology is about 0.78V, it comes that the value for R_0 is 1.63kΩ. This value is reduced to 1.2kΩ trading power consumption for better dynamics.

Since the reference voltage is self-biased there is a need for start-up circuit to prevent zero current state. Start-up circuit is designed with transistors MS0-MS2. If there is a zero current in the circuit the voltage at R_0 is low. This low state feeds the MS0/1 inverter which turns on MS2 and provides the low potential at the gates of PMOS MB11/12. This condition opens the path for the current to flow from power supply towards R_0. Consequently, voltage at the MB10 gate increases. Inverter triggers once again turning the MS2 off. It is important to emphasis that the size of MS0 should be much greater than the size of MS1. This way the overdrive voltage of MS0 is quite small, allowing inverter to trigger with lower voltage than $V_{DD}/2$. This ensures that inverter drives MS2 to cutoff.

The reset of the bias circuitry (MB0-MB8) serves to distribute generated reference to appropriate points. Transistors MB3-MB5 form high swing cascode current mirror biased with MB6/7 Sooch structure [10]. Transistors MB0 and MB1 are used in similar manner to bias M3/4.

C. Common Mode Feedback

OTA will be used within SC circuit driven with two non-overlapping, clocking signals at f_s sampling rate, named *Phi*1 and *Phi*2. Therefore, CMFB is accomplished with NMOS switches MC0-MC7 and four capacitors (two C_1 and two C_2) [11]. Transistor MC9 mirrors reference current while MC8 converts it into the voltage, V_{Nbias}, appropriate for biasing tail current source i.e. core transistor M0. Desired common-mode voltage is set slightly above $V_{DD}/2$ using sooch voltage divider, MR0-MR3. CMFB voltage, V_{CMFB}, is formed at the gate of core transistor, M0. Circuit's operation can be unveiled by analyzing charge transfer during two, non-overlapping phases. When *Phi*1 signal is active, switches MC0-MC3 are *off* and MC4-MC7 are *on*. In this case total charge on the capacitors is:

$$Q_{Phi1} = 2(V_{CM} - V_{Nbias})C_2 + (V_{OP} - V_{CMFB})C_1 + (V_{OM} - V_{CMFB})C_1. \quad (5)$$

During the second clock phase, *Phi*2 (MC0-MC3 *on* and MC4-MC7 *off*), total charge becomes:

$$Q_{Phi2} = (C_1 + C_2)(V_{OP} - V_{Nbias}) + (C_1 + C_2)(V_{OM} - V_{CMFB}). \quad (6)$$

Since charge in both clock phases has to be the same, net value of V_{CMFB} over two clock phases can be obtained by equating (5) and (6):

$$V_{CMFB} = \frac{V_{OP} + V_{OM}}{2} - V_{CM} + V_{Nbias} = V_{OCM} - V_{CM} + V_{Nbias}, \quad (7)$$

where V_{OCM} is the actual output common-mode voltage. If e.g. V_{OCM} starts to increases comparing to V_{CM} there is a small, positive increment superposed to ideal V_{Nbias} for biasing gate voltage of M0. Since M0 is common source stage in this signal path drain voltage of M0 decreases. Voltage drop at M0's drain is further transferred through two common-gate stages M1/2 and M3/4 opposing the initial V_{OCM} increase. Inverse reaction takes place if V_{OCM} deviates from V_{CM} in other direction. In this way negative feedback is formed which, over time, averages V_{OCM} to V_{CM}.

To determine adequate values for C_1 and C_2 capacitance two tradeoffs should be analyzed.

The first tradeoff puts bound on C_1 value. This capacitance is lumped together with OTA's load capacitance during active phase *Phi*1. Actually, OTA is only used during this phase for amplifying the input signal. At the same time desired common-mode voltage is sampled at C_2. This implies that C_1 capacitance value should be smaller than C_L in order not to deteriorate OTA dynamics. On the other hand its value should also be large enough to differ from MOS parasitic caps (particularly C_{gd}), otherwise stored charge, i.e. voltage, on it will not be preserved during the sampling period. Using SPICE analysis, C_{gd} capacitance of M5/6 and M3/4 output transistors is estimated to about 40fF, contributing in total with 80fF to the output node of OTA. Therefore, 500fF is adopted for C_1 as a tradeoff between MOS parasitic and loading effect of the OTA output.

Second tradeoff addresses C_2/C_1 ratio. During phase *Phi*2 the output common-mode voltage is corrected by tying C_1 and C_2 in parallel. Then the charge stored on these two capacitors will redistribute among each other equating the voltage on them. As a result the final voltage on parallel capacitance at the end of phase *Phi*2, V_{eq}, will be:

$$V_{eq} = \frac{k}{k+1}(V_{CM} - V_{Nbias}) + \frac{1}{k+1}(V_{OCM} - V_{CMFB}), \quad (8)$$

where $k = C_2/C_1$. Fig. 6 shows output common-mode voltage versus time for different values of k and sampling frequency f_s = 16.77 MHz.

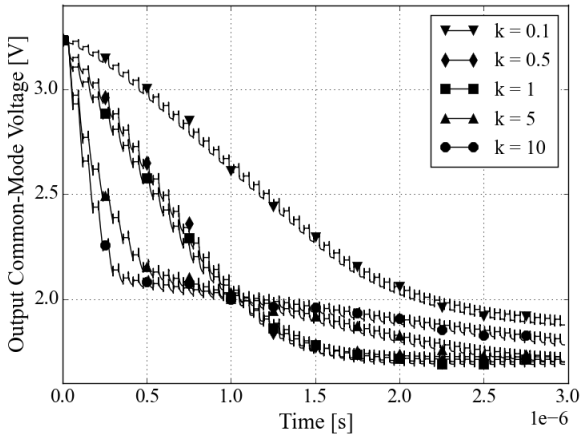

Fig. 6. Settling of output common-mode voltage.

The amount of CMFB voltage is tuned with C_2/C_1 ratio. First term in (8) represents well defined, fixed value, increment which is added to the unregulated, second term.

For $k > 1$ (i.e. $C_2 > C_1$) first term dominates, increments are larger and the output common-mode stabilization is expected to be obtained sooner. However these large increments usually force output to slew resulting output to actually settle later. For $k < 1$ increments are smaller and output common-mode stabilization comes later in time but in more controlled manner. One can clearly see that there is a tradeoff between settling of output voltage around desired common-mode value, slewing and the amount of CMFB applied. As a result of this tradeoff k=1 i.e. C_2 = 500fF is chosen. Also, it can be concluded that k= 0.5 gives similar response and even smaller value for C_2 capacitance (250fF). Still, this value approaches parasitic capacitances jeopardizing first tradeoff mentioned earlier.

III. Simulation Results

Circuit's behavior is examined through set of various simulations in SPICE. Results for nominal PVT (Process, Voltage, Temperature) conditions at room temperature are summarized in Table III.

TABLE III
SIMULATED OTA CHARACTERISTICS

Param.	Description	Condition	Value
A_0	DC, open loop gain	open loop/closed loop[a]	57.6 dB
Φ_M	Phase margin	open loop/closed loop	83 °
f_{GBW}	Gain-bandwidth	open loop closed loop	140 MHz 126 MHz
SLR	Slew rate	closed loop, excitation:	190 V/μs
t_S	Settling time	pulse, ±(*ICMR*/2) V, 100kHz	16.6 ns
V_{OMAX}	Maximum output swing	closed loop, excitation: sine, ± 3.3 V, 1MHz	± 1.83 V
PSRR	Power supply rejection ratio	open loop, from V_{DD} open loop, from V_{SS}	215 dB 218 dB
CMRR	Common-mode rejection ratio	open loop, from V_{CM}	240 dB
ICMR	In. common-mode range	open loop closed loop	4 mV 2.54 V
OCMR	Out. common-mode range	open loop closed loop	1.92 V 2.74 V
V_{OCM}	Out. common-mode voltage	open loop/closed loop	1.7 V

[a]Unity gain feedback configuration

As can be seen from Table III, target design requirements concerning open loop gain, gain-bandwidth and slew rate are met. It can be also noted that circuit is slightly overdesigned. This is to leave some margin for PVT variations and noise which will inevitable arise at layout/physical level.

Even open loop analysis confirms stability it is of curtail importance to check circuit's closed loop behavior. This is done by using famous Middlebrook method, where instead open loop, total loop gain is examined [11]. Results are graphically presented in Fig 7.This method is considered to be the most trustable when examining stability of feedback systems. It is also favorable because there is no need to break feedback loop hence bias points are not corrupted.

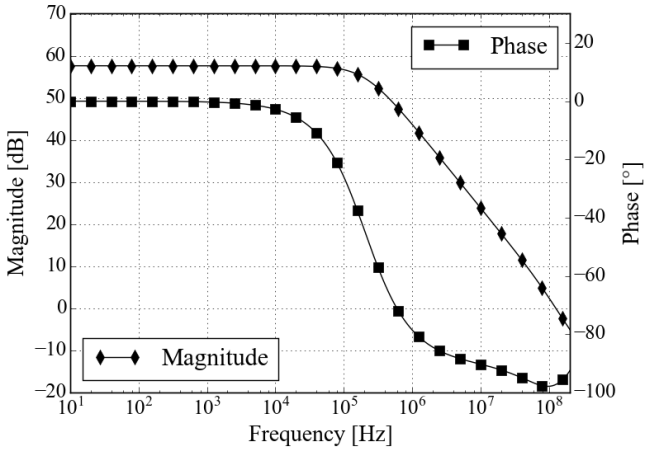

Fig. 7 Total loop gain (Magnitude and Phase) versus frequency.

Usually leading CAD vendors, implement this method into its simulation software (e.g. Cadence® Spectre, *iprobe* component in conjunction with *stb* simulation directive). Nevertheless, diving into the [12] one can build its own SPICE deck for implementing the method.

Good circuit dynamics are paid with burning extra power. Total power of the circuit is quite high and it is estimated to P_{TOT}= 9.77mW. Since fully differential, power-supply and common-mode rejection ratios are quite high as expected. Usage of high swing bias cascodes resulted with satisfactory output swing.

IV. Conclusion

This paper presents one design example of OTA circuit considering CMOS 350nm technology process. Designed circuit is to be integral pat of ΔΣ ADC. Adopted architecture is discussed with emphasis on individual sub-blocks namely: Core, Common-Mode Feedback and Bias with start-up. Design procedure of each sub-block is given, as well. For this purpose a set of useful curves is extracted using SPICE giving the insight into MOS device behavior in target technology process. Important design tradeoffs are drawn based on those curves. Transistor level simulation results are presented and discussed. Based on these results one can conclude that circuit meets severe dynamic requirements while preserving stability. Consequently power consumption is increased hence design could be further optimized in this direction.

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