The Decomposition of DSP's Control Logic Block for Power Reduction

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***Abstract*—The paper considers the architecture and low power design aspects of the digital signal processing block embedded into a three-phase integrated power meter IC. Utilized power reduction techniques were focused on the optimization of control logic block. The operations that control unit performs are described together with power optimization results.**

***Index Terms*—Digital signal processing, power optimization.**

I. Introduction

NOWADAYS, most of electronic devices which are used for the measurement of power line parameters relays on single chip referred to as integrated power meter (IPM). An IPM usually embeds powerful digital signal processor block (DSP) performing various data-intensive calculations. This paper proposes a DSP core used in power metering applications, which enables high performances at the levels as those obtained with commercial DSP microprocessors, and, at the same time, operates at significantly reduced power consumption.

The paper explains the operations performed by DSP used for processing the instantaneous values of current and voltage signals including the digital filtering methods. The DSP calculates root mean square values of voltage and current, active, reactive, apparent power and energy. Besides, new circuit for distortion power measurement is presented.

Power dissipation is an important part of system-on-chip (SoC) design specifications. Low power design techniques, with an emphasis on modern standard cell technologies, are applied to the design of a DSP core. Effort is put into the dynamic power minimization. Since DSP's control unit is one of largest and most power consuming DSP's part, the paper presents the utilized low power techniques which are mainly focused on the optimization of control logic block.

The operation of DSP is discussed in the following section of the paper. Then, in Section three, the architecture of the proposed core is given, with the description of utilized low power techniques. The implementation results are given in Section four.

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II. DSP's Operation

The proposed DSP circuit is incorporated into an IPM chip, the mixed-signal circuit consisting of analog and digital signal processing blocks. The analog part of IPM contains Sigma-Delta AD converters [1] for current and voltage signal conversion into digital words, Band-Gap voltage reference and PLL circuits.

The digital part is composed of digital filters [2], DSP block and 8052 microcontroller unit. From AD converters and digital filters [2] the DSP gets 16-bit digital samples of instantaneous voltage, current and phase-shifted voltage signals at data-rate of 4096 samples per second. Based on values of current and voltage, DSP calculates root-mean square (RMS) values of current I_{RMS}, and voltage V_{RMS}, active power P, reactive power Q, apparent power S and power-factor $cos(\varphi)$ every second. The measurement range for current signal is from 10mA RMS to 100A RMS, and for voltage it is up to 300V RMS. Besides, DSP measures the instantaneous value of the power-network frequency with a maximum error of 0.01 Hz.

The measurement results are obtained for all three power line phases and three distinct result sets are provided, each dedicated to specific power line phase.

A short survey of used equations that explains the DSP's operation would be as follows.

A. The used equations

The instantaneous value of current, as function of time, can be represented in the form:

$$i(t) = \sqrt{2} I_{RMS} \cos(2\pi f t + \varphi) \quad (1)$$

After the discretization in time domain, it becomes:

$$i(n) = \sqrt{2} I_{RMS} \cos(n \cdot 2\pi f / fs + \varphi), \quad (2)$$

where f represents the power-line signal frequency equal to 50Hz, and fs is the AD converter sampling frequency, equal to 4096Hz.

Root-mean-square, I_{RMS}, is calculated once per second according to the expression (3):

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$$I_{RMS} = \sqrt{\frac{\sum_{n=1}^{N} i(n)^2}{N}} \quad (3)$$

The DSP calculates new I_{RMS} value every second and value of parameter N in (3) is equal to 4096. Similar expression, like for I_{RMS}, is used for V_{RMS} calculation.

$$V_{RMS} = \sqrt{\frac{\sum_{n=1}^{N} v(n)^2}{N}} \quad (4)$$

If the instantaneous values of current and voltage are as follows,

$$i(t) = \sqrt{2} I_{RMS} \cos(2\pi ft + \varphi_1) \quad (5)$$

$$v(t) = \sqrt{2} V_{RMS} \cos(2\pi ft + \varphi_2) \quad (6)$$

the instantaneous active power *p(t)* is:

$$p(t) = i(t) \cdot v(t) \quad (7)$$

After the discretization of the instantaneous power, the active power *P* is calculated according to:

$$P = \frac{\sum_{n=1}^{N} p(n)}{N} \quad (8)$$

The instantaneous reactive power *q(t)* is obtained by multiplying current and phase-shifted voltage signals.

$$i(t) = \sqrt{2} I_{RMS} \cos(2\pi ft + \varphi_1) \quad (9)$$

$$v_p(t) = \sqrt{2} V_{RMS} \cos(2\pi ft + \varphi_2 + \pi/2) \quad (10)$$

The reactive power *q(t)* is

$$q(t) = i(t) \cdot v_p(t) \quad (11)$$

The average reactive power *Q* is calculated according to:

$$Q = \frac{\sum_{n=1}^{N} q(n)}{N} \quad (12)$$

Apparent power *S* and power factor *cos(φ)* are calculated according to (13) and (14):

$$S = I_{RMS} \cdot V_{RMS} \quad (13)$$

$$\cos(\varphi) = P/S \quad (14)$$

$$S^2 = P^2 + Q^2 + D^2 . \quad (15)$$

The relation (15) between apparent power *S,* active power *P*, reactive power *Q* and distortion power *D*, suggests us that it is enough to calculate *P*, *Q* and *S* and then use the (15) to find the distortion power *D*.

Possible sources of error in active power *P* calculation are the phase difference between voltage and current values and the fact that power-network frequency is slightly changed round the nominal (50Hz), so there are not an integer number of voltage half-periods in a second. Error eliminating is necessary, so after the multiplication of the current and voltage values, the values $i^2(t)$, $v^2(t)$, *p(t)* and *q(t)* are filtered, accumulated 4096 times per second and the achieved total is divided with 4096 every second.

III. DSP'S ARCHITECTURE

A. Controller/datapath architecture

The architecture of DSP [3], [4] utilizes controller/ datapath architecture and consists of several blocks:

- Block 1 – the part which consists of arithmetical units used for I^2, V^2, *P*, *Q* accumulating and energy calculation
- Block 2 – including arithmetical operators used for calculation of current and voltage RMS, power factor, active, reactive, distortion and apparent power
- Block 3 – control unit that controls all other parts of DSP.
- Block 4 – frequency measurement circuit
- Block 5 – RAM memory block storing the measurement results.

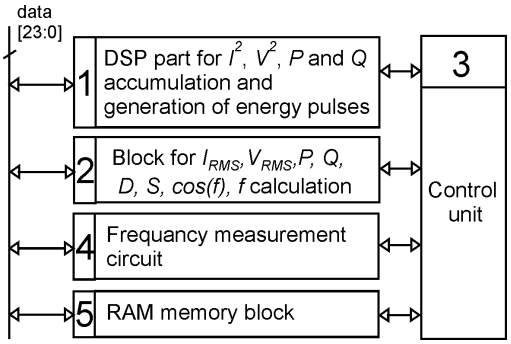

Fig.1. DSP block diagram.

There is a single 24-bit data bus connecting these sub-blocks of DSP. The control path of DSP unit (Block 5) is implemented as a finite state machine (FSM) that generates a number of control signals. These signals determine what component can write to 24-bit data, what registers are loaded from the bus and what arithmetical operation is performed.

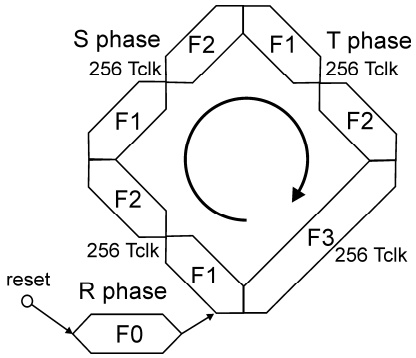

Fig.2. The FSM state sequence.

During DSP's measurement operation, the control unit periodically executes main state sequence that lasts 1024 clock periods [5], repeated 4096 times during the time interval of one second. The sequence is divided into four sub-sequences called R, S, T and E that lasts 256 clock periods each. The first three sub-sequences R, S and T control the calculations made for each phase of the three-phase energy system. The fourth sub-sequence, denoted E, manages the calculations that are periodically repeated every second [5].

The control unit is composed of four smaller finite state machines: named F0, F1, F2 and F3. The reason for dividing the control unit is significant power consumption reduction which will be examined in following sections. Two sub-

FSMs, F1 and F2, perform arithmetical operations within the Block1 during the phases R, S and T, while sub-FSM F3 - performs operations within Block 2 during E period. The F0 is intended for RAM memory initialization and F0 is active only at the beginning of chip operation, after the main reset state. The operations that F1, F2 and F3 perform will be described in detail.

B. The operation of F1

The FSM F1 executes the state sequence during phases R, S and T and consists of one hundred and two different states. It is used for processing the squared value of instantaneous current and voltage AC signals (necessary for obtaining I_{RMS} and V_{RMS}) and instantaneous values of active and reactive power.

The operation sequence for current square accumulating is given in Fig. 3. The sequence is performed 4096 times every second.

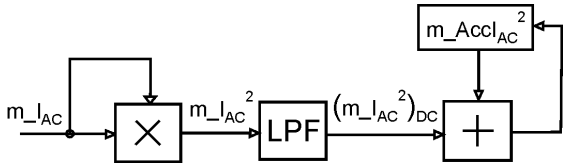

Fig. 3. Data processing chain for current-square accumulation.

At the beginning of the F1 operation sequence, the AC part of instantaneous current signal i_{AC}, stored in the 24-bit RAM register m_I_{AC}, is squared in the multiplication unit, which belongs to the Block1. Then, the squared value i_{AC}^2 is passed through the digital Low pass filter (LPF), and after, the DC value of squared value i_{AC}^2 signal, is accumulated into the 48 bit accumulation register $m\_AccI_{AC}^2$. The register is stored in RAM memory and consists of two 24-bit register parts.

The LPF is implemented as a filter with Infinite impulse response (IIR) and helps in reducing the I_{RMS} calculation error. This error could exist because the time interval of one second (that is, accumulating time of i_{AC}^2value) is not always equal to the integer number of power-line-signal half-periods.

The LPF takes at inputs the squared value i_{AC}^2, which is stored in the register $m\_I_{AC}2$, and produces at output the DC value of i_{AC}^2. The LPF has cut-off frequency of 10Hz and its transfer function is given by (16).

$$H_{LPF}(z)=\frac{(m\_I_{AC}^{\ 2})_{DC}}{m\_I_{AC}^{\ 2}}=\frac{2^{-6}}{1-z^{-1}(1-2^{-6})} \tag{16}$$

The transfer function $H_{LPF}(z)$ can be easily transformed into the equations in which the operands are expressed by registers:

$$(\mathrm{m\_FI^2_{AC}x64})_{\mathrm{NEW}}=\mathrm{m\_FI^2_{AC}x64}\cdot(1-\frac{1}{2^6})+\mathrm{m\_I^2_{AC}} \tag{17}$$

$$(\mathrm{m\_I^2_{AC}})_{\mathrm{DC}}=(\mathrm{m\_FI^2_{AC}x64})/64 \tag{18}$$

The 48-bit LPF filter register $m\_FI^2{}_{AC}x64$, used in (2) and (3), consists of two 24-bit parts that are stored in the RAM memory block. The register contains the DC value of signal i_{AC}^2, multiplied by constant number 64.

The operations described by (2) and (3) are done by arithmetical circuits within the Block 1, which structure is given in Fig. 4, and includes one multiplication unit and one circuit for addition and subtraction. The intermediate results of operations (i_{AC}^2 and the DC value of i_{AC}^2) are temporarily stored in the registers RegA and RegB of Block1 (Fig.1). Only the AC part of instantaneous current signal i_{AC} (register m_I_{AC}) accumulation register $m\_AccI_{AC}^2$ and LPF filter register $m\_FI^2{}_{AC}x64$ are located in RAM.

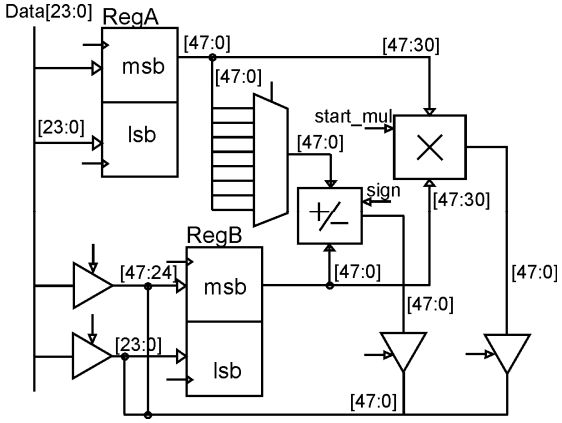

Fig. 4. The structure of Block 1.

The FSM sequence of operations for the accumulation of squared current values is given by the Fig. 5. The sequence consists of simple data transfer, shifting, multiplication and addition operations, performed at registers RegA and RegB.

$$\mathrm{m\_I_{AC}} \rightarrow \mathrm{RegA\_h, RegB\_h}$$
$$\mathrm{RegA\_h} \times \mathrm{RegB\_h} \rightarrow \mathrm{RegA}$$
$$\mathrm{m\_FI^2_{AC}x64\_h} \rightarrow \mathrm{RegB\_h}$$
$$\mathrm{m\_FI^2_{AC}x64\_l} \rightarrow \mathrm{RegB\_l}$$
$$\mathrm{RegA - (RegB >> 6)} \rightarrow \mathrm{RegA}$$
$$\mathrm{RegA + RegB} \rightarrow \mathrm{RegA}$$
$$\mathrm{RegA\_h} \rightarrow \mathrm{m\_FI^2_{AC}x64\_h, RegB\_h}$$
$$\mathrm{RegA\_l} \rightarrow \mathrm{m\_FI^2_{AC}x64\_l, RegB\_l}$$
$$\mathrm{m\_AccI^2_{AC}\_h} \rightarrow \mathrm{RegA\_h}$$
$$\mathrm{m\_AccI^2_{AC}\_l} \rightarrow \mathrm{RegA\_l}$$
$$\mathrm{RegA + (RegB >> 6)} \rightarrow \mathrm{RegA}$$
$$\mathrm{RegA\_h} \rightarrow \mathrm{m\_AccI^2_{AC}\_h}$$
$$\mathrm{RegA\_l} \rightarrow \mathrm{m\_AccI^2_{AC}\_l}$$

Fig. 5. The sequence of accumulation of squared current values.

The similar procedure is performed by Block 1 for processing the squared value of instantaneous voltage AC part signal – v_{AC}^2 (necessary for obtaining V_{RMS}) and instantaneous values of active p and reactive power q. The results are stored in the RAM registers: $m\_AccV_{AC}^2$, m_AccP

and m_AccQ. The difference is in used multiplication operands: the voltage samples are multiplied to obtain V_{RMS}; voltage and current sample values for active power, and current-sample value is multiplied with phase-shifted voltage-sample for reactive power processing.

C. The operation of F2

The F2 is active during phases R, S and T and generates the energy pulses for measured active and reactive energy. The FSM consists of one hundred and ninety three states. A pulse is generated when measured energy exceeds predetermined energy level. The default energy level is one Watt-hour for active and VAR (Volt-Ampere reactive) for reactive energy.

The DSP has four outputs producing the narrow pulses: Ea_pos – for consumed active, Ea_neg – generated active, Eq_pos – inductive reactive, and Eq_neg – capacitive reactive energy. The energy level is stored in m_Whr register, the part of RAM memory block, and can be modified. The operations are carried out by Block 1 using the adder/subtractor and registers RegA and RegB.

The sequence of operations is given in Fig.6. At the beginning of each sequence, performed exactly 4096 times during the time interval of one second, the active power value m_P, is added to the value of 48-bit register m_AccEa. The m_AccEa consists of two parts: the MSB part - m_AccEa_h and the LSB part - m_AccEa_l, both stored in RAM. After addition operation is done, the value of m_P and new value of m_AccEa are compared with zero. If value of m_P is positive and if new value of m_AccEa is greater than the energy level equivalent (given by m_Whr), a pulse on Ea_pos is generated and m_AccEa is subtracted by the m_Whr value. Else, if both m_P and m_AccEa are negative, a pulse on Ea_neg is generated, and value of m_Whr is added to m_AccEa.

The similar procedure stands for the reactive energy processing. Accompanied registers are m_AccEq_h and m_AccEq_h.

Besides dealing with energy pulses, the F2 eliminates DC offsets from instantiations current and voltage signals that are derived from digital filters. This is necessary for the calculation of current and voltage RMS value. The DC offset will give a additional DC component after squaring operation. Since this DC component is extracted by LPF, this offsets can induce the error to RMS values. This problem is avoided by introducing the HPF in voltage and current signal processing chains. The HPF, applied to instantaneous current and voltage signals, is implemented as IIR digital filter with cut-off frequency 5Hz and transfer function as given by:

$$H_{HPF}(z) = (1-2^{-10})\frac{(1-z^{-1})}{1-z^{-1}(1-2^{-9})} \tag{19}$$

$m\_P \rightarrow RegB\_l$
$m\_AccEa\_h \rightarrow RegA\_h$
$m\_AccEa\_l \rightarrow RegA\_l$
$RegA + RegB \rightarrow RegA$
if (RegB > 0) {
  $m\_Whr \rightarrow RegB\_l$
  if ((RegA - (RegB << 12)) > 0) {
    $RegA - (RegB << 12) \rightarrow RegA$
    genarate pulse for positive Ea;
  }
} else {
  if (RegA < 0) {
    $m\_Whr \rightarrow RegB\_l$
    $RegA + (RegB << 12) \rightarrow RegA$
    genarate pulse for negative Ea;
  }
}
$RegA\_h \rightarrow m\_AccEa\_h$
$RegA\_l \rightarrow m\_AccEa\_l$

Fig. 6. The sequence of operations producing the energy pulses on Ea_neg and Ea_pos pins.

The HPF transfer function can be transformed into the equations (20) and (21) performed by DSP.

$$(m\_FIx1024)_{NEW} = m\_FIx1024(1-\frac{1}{2^9}) + (2^{10}-1)(m\_I - m\_I\_p) \tag{20}$$

$$m\_I_{AC} = m\_FIx1024/1024 \tag{21}$$

The following registers values are used in the equations (20) and (21):

- m_I and m_I_p – two consecutive current samples obtained directly from digital filters
- m_FIx1024 is 48-bit HPF register, which contains the AC value of *i(t)*, multiplied by constant value 1024. The register consists of two parts: the MSB part – m_FIx1024_h and LSB part - m_Fix1024_l.
- m_I_{AC} is AC part of instantaneous sample of current signal. It represents the result of filtering operation and it is further used by FSM F1.

The operation sequence for the offset elimination, performed by F2, is given in the Fig. 8. The operations are carried out by Block 1.

The similar procedure is made for processing of m_V_{AC} (necessary for obtaining V_{RMS}). The intermediate results are stored in 24-bit RAM registers: m_FVx1024_h and m_FVx1024_l.

$$m\_I\_p \rightarrow RegA\_l$$
$$m\_I \rightarrow RegB\_l$$
$$RegA\_l - RegB\_l \rightarrow RegA\_l$$
$$RegA \rightarrow RegB$$
$$RegA - (RegB << 10) \rightarrow RegA$$
$$m\_FIx1024\_h \rightarrow RegB\_h$$
$$m\_FIx1024\_l \rightarrow RegB\_l$$
$$RegA + RegB \rightarrow RegA$$
$$RegA - (RegB >> 9) \rightarrow RegA$$
$$RegA\_h \rightarrow m\_FIx1024\_h$$
$$RegA\_l \rightarrow m\_FIx1024\_l$$
$$RegA \rightarrow RegB$$
$$0 \rightarrow RegA\_l$$
$$RegA + (RegB >> 10) \rightarrow RegA$$
$$RegA\_l \rightarrow m\_I_{AC}$$

Fig. 7. The sequence for high pass filtering of instantiations current sample signals, done by F2.

D. The operation of F3 FSM

The fourth sub-sequence of the control unit manages the calculations that are periodically repeated every second and consists of three hundred and four states.

Based on accumulating sums $m\_AccI_{AC}^2$, $m\_AccV_{AC}^2$, m_AccP and, m_AccQ, arithmetical operations are performed by Block 2 to generate voltage and current root mean square values m_I_{RMS} and m_V_{RMS} and mean active and reactive power values m_P and m_Q. The sequence of operations is performed by FSM F3.

The interior structure of Block 2 is given in Fig. 8. It consists of two registers named RegC and RegD and arithmetical units that implement square rooting, subtraction, multiplication and division.

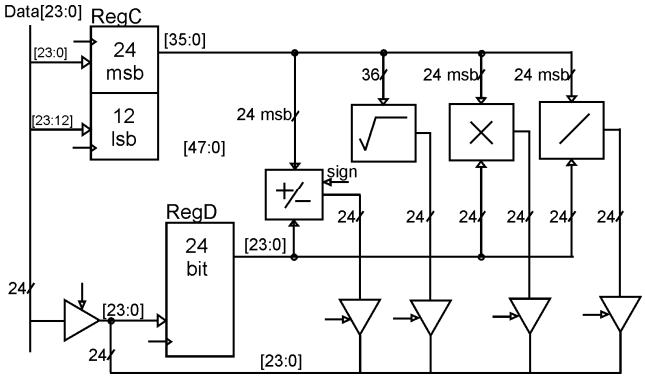

Fig.8 The structure of Block 2

The sequence, controlled by F3 that generates current root mean square m_I_{RMS}, is given in Fig. 9.

To generate value m_I_{RMS}, accumulated sum $m\_AccI_{AC}^2$ is stored into RegC and then, it is divided by 4096. Next, square rooting operation is performed over the average value of voltage square. Then, current offset $m\_I_{AC}off$ is subtracted,

$$m\_AccI^2\_h \rightarrow RegC\_h$$
$$m\_AccI^2\_l \rightarrow RegC\_l$$
$$\sqrt{RegC} \rightarrow RegD$$
$$0 \rightarrow m\_AccI^2$$
$$m\_I_{ACoff} \rightarrow RegC\_h$$
$$RegC\_h - RegD \rightarrow RegD$$
$$m\_Igain \rightarrow RegC\_h$$
$$RegC\_h \times RegD \rightarrow RegD$$
$$RegD \rightarrow m\_I_{RMS}$$

Fig. 9. The sequence that generates current root mean square m_I_{RMS}.

multiplied with gain correction m_Igain and root mean square of current is obtained (Fig. 9).

The similar processing steps are conducted for m_V_{RMS}. For mean active and reactive power calculation the square root calculation is avoided. Apparent power m_S is obtained by multiplying m_I_{RMS} and m_V_{RMS}, and power factor m_CosF – by dividing active m_P and apparent power m_S.

In addition to finding mean active (m_P), reactive (m_Q) and apparent power (m_S), the distortion power [6] (stored in the register m_D) calculation is provided. F3 controls the operations producing the m_D. Arithmetical operators used to calculate the value of m_D, belong to blocks 1 and 2. The structure of Block 1 had to be slightly modified. The new input is introduced to RegB (the part of Block 1) which makes the connection from the multiplication unit from Block 2. The result of multiplication operation, done by arithmetical operator within Block2, has to be transferred to the RegB. The sequence is given in Fig. 10.

At the beginning, the register RegA is reset to zero, and the content of register m_S is copied to both of the registers RegC and RegD. The squaring operation is performed and the result is moved to the RegA. Then, the active power m_P is moved to RegC and RegD, and the multiplication is performed. The result is subtracted from register RegA. The same operations

$$0 \rightarrow RegA\_h, RegA\_l$$
$$m\_S \rightarrow RegC\_h, RegD$$
$$RegC\_h \times RegD \rightarrow RegB$$
$$RegA + RegB \rightarrow RegA$$
$$m\_P \rightarrow RegC\_h, RegD$$
$$RegC\_h \times RegD \rightarrow RegB$$
$$RegA - RegB \rightarrow RegA$$
$$m\_Q \rightarrow RegC\_h, RegD$$
$$RegC\_h \times RegD \rightarrow RegB$$
$$RegA - RegB \rightarrow RegA$$
$$RegA \rightarrow RegC$$
$$\sqrt{RegC} \rightarrow RegD$$
$$RegD \rightarrow m\_D$$

Fig. 10. The sequence that generates distortion power m_D.

are done with the value m_Q. After, the content of RegA is moved to the RegC, and square root operation is performed. Finally, the result is moved from RegD into the m_D, which is stored in the RAM memory.

IV. The Implementation Results

Dynamic power dissipation of DSP block can be divided into three main areas: power consumed by memory blocks, arithmetical operators and by clock tree nets.

The first area is the power cost associated with accesses to the three data memories (represented by Block 5 in the Fig. 1). It is well known that memory accesses can form the largest component of power consumption in data-dominated applications. The power is consumed within the RAM units themselves, and also, during data transmission across the large capacitance of the 24-bit data bus. The control unit was modified to decrease the number of accesses to the RAM memory. Besides, the datapath was changed that the intermediate results, that DSP calculates, are stored in working registers of Block 1 and 2. Only the final measurement results are saved in RAM.

The second main area of power consumption comes from the energy dissipated in performing the actual operations on the data. This is made up of the energy dissipated by transitions within the datapath associated with the data (Block 1 and 2), and the control overhead (Block 3) required to perform the operations. In the proposed DSP, the most of dissipated power comes from large control unit and its power reduction will be further described.

Clock power is the third component of signal processing block power because the clock is fed to most of the circuit blocks in the processor and the clock switches every cycle. Considering all clock signals, the total clock power is a substantial 30% of the DSP's power. Clock gating is the efficient technique for dynamic power reduction. To avoid glitches, beside AND circuits, the level sensitive latches are used for clock gating circuit implementation.

The datapath of DSP incorporates several arithmetical units for multiplying, dividing and square rooting which are realized as sequential circuits. Since arithmetical blocks are not used all the time, their clock trees can be gated, reducing the power consumption. The DSP design was further power optimized. The gating signals are the only way to write data into registers and memory blocks. For example, the clock signals of registers in the Block 1 and Block 2 were gated.

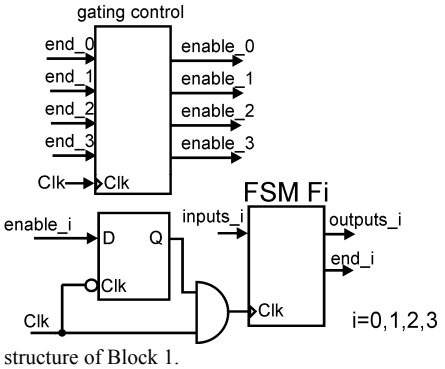

Fig. 11. The structure of Block 1.

The rest of the optimization process considered the DSP's control unit. The control unit incorporates over six hundred states and required huge combinational logic within the synthesized FSM. The implementation of control logic block occupies large portion of DSP's area. Also, it represents one of the largest power consumers among DSP's blocks.

The following power minimization techniques were used: FSM decomposition [7, 8], clock gating and Grey code encoding [9]. The first technique divides large control unit into several smaller state machines, simplifying their combinatorial logic blocks. The division of control unit into smaller state machines has positive effect on power dissipation. After, the clock gating technique was used. The clock gating disables inactive parts of FSM by stopping its clock signal, and, reduces the switching activity within the combinatorial logic blocks. At the end, Gray binary encodings are assigned to the FSM's states to further reduce the power.

During FSM decomposition the transition graph of original FSM was considered first, and after, divided into four sub-graphs. Four sub FSMs were created, named with F0, F1, F2 and F3, which jointly produce the equivalent behavior as the original FSM. The decomposition is performed considering the datapath architecture. The states within one subset control the arithmetical operations performed by same part of DSP. For example, F1 and F2 perform the operations executed by Blocks 1 and 2, and state machine F3 - the operations done by Block 2.

After the FSM decomposition is done, the clock gating is introduced in the control unit implementation. The gating control circuit (shown in Fig. 11) is added to the control logic block. New circuit identifies the currently active FSM and enables the clock input signals to the active FSMs. When the clock signal is present at the input of active FSM, the other three state machines are blocked.

The DSP block was implemented in technology AMI CMOS 350nm with power supply voltage of 3.3V. The Cadence tools were used for implementation. First, the design was verified by RTL simulation, and synthesized by using

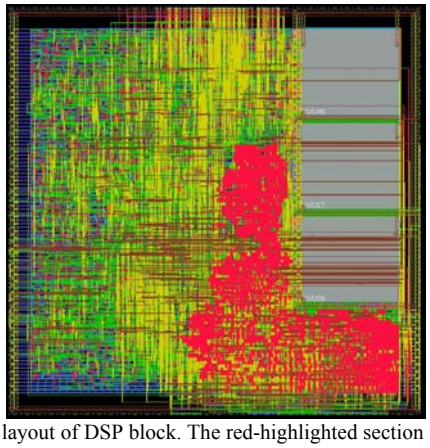

Fig. 12. The layout of DSP block. The red-highlighted section represents the area of huge control logic unit.

Cadence's RTL Compiler. Then, SoC Encounter has performed floor-planning, placement, routing, and clock and reset trees generation. At the end of logical verification process, the Verilog file was extracted from layout and brought back to NCsim simulator where final check of the total digital part of the IC was performed. During the post-layout simulation, switching activity file was obtained and the power consumption results are obtained by the SoC Encounter taking account the parasitic capacitances from layout and switching activity file.

The estimation of DSP's power consumption gave the valuable information about the energy budget and identified all power hungry components. Three power analyses were performed: for the: (a) original design (before the power minimization techniques where applied), (b) DSP design which is optimized by only gating and FSM decomposition, and finally, (c) design where all proposed techniques were applied: FSM decomposition, clock gating and Gray state encoding. The Table I gives the simulated power consumption values of different DSP cores, derived after layout generation. The power consumption of not optimized design was 1.82mW. When all these techniques were applied, the total power became only 1.043mW resulting in the 42% switching power reduction, compared to the non-optimized implementation.

TABLE I
THE RESULTS OF POWER OPTIMIZATION

Symbol	Not optimized	Decomposition & clock gating [a]	Decomposition, clock gating & Grey encoding
Area	1.84mm^2	1.831mm^2	1.823mm^2
Clock tree power	0.732mW	0.263mW	0.227mW
Control unit power	0.407mW	0.172mW	0.172mW
DSP's power	1.82mW	1.117mW	1.043mW

V. CONCLUSION

The architecture and the low power design aspects of the digital signal processing block embedded into a three-phase integrated power meter IC, are considered. The operations that control unit performs are described together with power-optimization results.

The power reduction techniques were successfully implemented on the optimization of the control logic block. The control unit of DSP block, implemented as finite state machine, was decomposed into four smaller state machines, clock gating was completely introduced and Gray finite state machine encoding used. The resulting effect was the significant reduction of the power consumption.

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