Pattern-Based Approach to Current Density Verification

Vazgen Melikyan, Eduard Babayan, and Ashot Harutyunyan

***Abstract*—Methodology of static verification of current density based on layout patterns common in IC designs is proposed. The methodology is based on pre-calculation of current density distribution for common layout patterns. Then using the obtained data to calculate current densities of large circuits by partitioning them to selected patterns. Presented experimental results show the effectiveness of the approach.**

***Index Terms*—Current density, electromigration, verification, patterns.**

I. Introduction

With increasing technology scaling, physical effects consideration and their impact priorities have changed. In particular, impact of electromigration (EM) increased [1-4]. EM is the mass transport in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms [1]. This effect damages interconnect because amounts of matter leaving and entering a given volume of interconnect are not equal, leading to accumulation or loss of material which results in damage [1]. When atomic flux into a region is greater than the flux leaving it, the matter accumulates in the form of a hillock. If the flux leaving the region is greater than the flux entering, the depletion of matter ultimately leads to a void (Fig. 1) [2].

Obviously, EM results in failure of IC which can be result not only of break or short-circuit, but also a significant increase in the interconnect resistance.

EM is defined as [3]:

$$J = -\frac{N_A}{kT} D_0 e^{-\frac{Q}{kT}} eZ^* \rho j \quad (1)$$

where N_A – density of atoms in the crystal lattice; D_0 – diffusion coefficient; Q – activation energy; eZ^* - resulting charge; ρ - resistivity; k – Boltzmann constant; T – absolute temperature; j – current density.

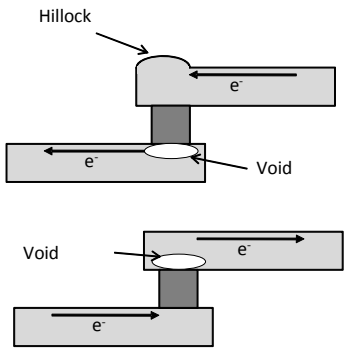

Fig. 1. Hillocks and voids.

During IC design it is required to check design against EM vulnerabilities. As it is seen from (1), such a check can be done by checking current density in interconnect against maximum allowable current density. Currently there are different current density verification EDA tools by different vendors. These tools have common disadvantages: they work only on chip level, require additional extraction and simulation steps, require large amount of background information, lack error correction, etc. [4,5]

This paper presents methodology of creation of current density verification tool based on common layout patterns which enables high verification performance without need of additional extraction and simulation steps.

II. Methodology

It is proposed to select common layout patterns (LP) (Fig. 2), taking into account the frequency of their use in real

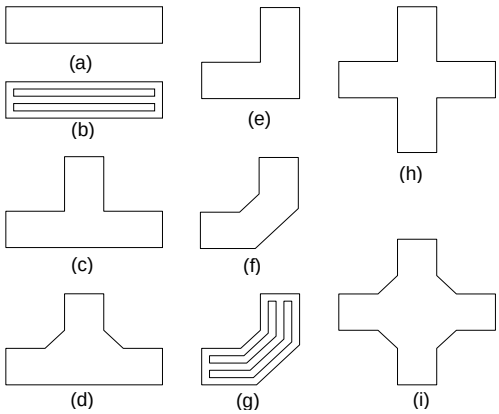

Fig. 2. Common layout patterns selected for modeling.

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TABLE I
STATISTIC DATA FOR PATTERNS SELECTION

LP	IC A		IC B		IC C		IC D	
	Area, %	Count	Area, %	Count	Area, %	Count	Area, %	Count
a.	39	16643910	36	20582714	40	7374407	31	6583941
b.	10	9283	14	16700	0	0	0	0
c.	4	56859	2	13269	9	170152	5	8195
d.	0	0	4	2582	0	0	0	0
e.	16	341139	4	840437	11	166584	15	225007
f.	0	0	12	38474	2	39033	0	5
g.	1	28	1	56	0	0	0	64
h.	3	65401	3	26780	6	95161	2	16339
i.	0	0	5	1341	0	0	0	0
Total	73		81		68		53	

ICs and relative areas covered by them statistically (Table I).

Simulation of these patterns enables estimation of maximum current density in these patterns depending on their geometrical parameters.

For LP selection current density values in the direction of the normal were taken as boundary conditions. The dependence of the maximum current density on the boundary conditions and geometric parameters of the model was calculated.

The essence of the method is demonstrated below for the sample LP (Fig. 3). In this case currents distribution is uniform in the direction of normal, equal to j_n and $-j_n$ for

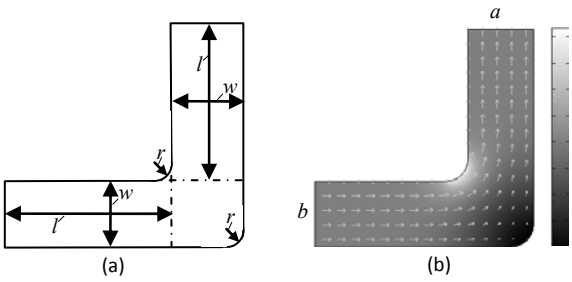

Fig. 3. For modeled LP: a – parameters; b – current density distribution.

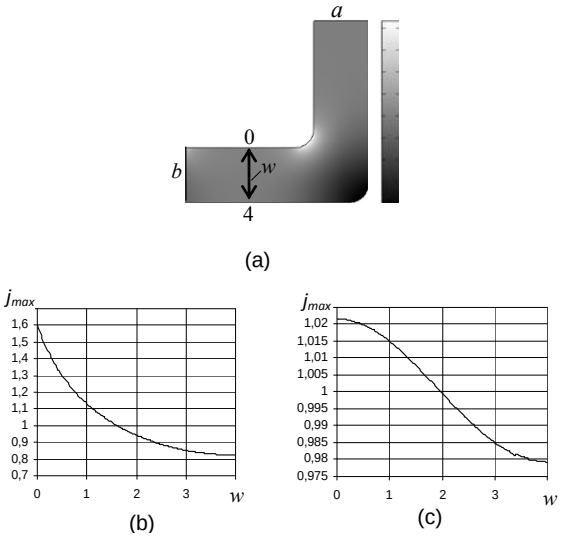

Fig. 4. Uneven distribution of boundary currents.

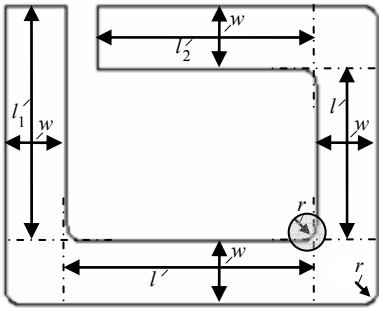

Fig. 5. The selected structure to obtain l_{min}.

edges *a* and *b* respectively, and 0 for the rest. Current density distribution map shows that in the inner corner of the LP current is thickened, and on the outside, on the contrary, is diluted. Simulation was performed to identify patterns of current distribution for non-uniform boundary conditions.

For edge *a* of LP in Fig. 4a, a boundary condition of uniform current distribution $j_n=1$ was set. Current distribution for edge *b* is shown on Fig.5b and it is mostly concentrated in upper corner. Current density reduces near upper corner and increases near bottom at a distance from edge *b*. In the middle of the straight segment the densities of these currents are most close to each other (Fig. 5c).

It was found out that with the increase of length of LP branches, the largest and smallest values in Fig.4c tend to 1. Consequently, it can be assumed that when length of branches *l* decreases in the considered model, the impact of boundary conditions distribution on the largest value of current density (LVCD) decreases. This allows neglecting boundary conditions distribution and its impact on current density distribution. The calculation of the boundary currents distribution leads to solution of differential equations. It is required to find a minimum length of branches l_{min} such that for branches with larger lengths, the relative difference between the maximum values of current density does not exceed the specified error ε at all possible *r* and *w*.

The length l_{min} should be found for boundary condition, assumed as such from a specific practical point of view. There could be other conditions at which smaller values of l_{min} are obtained for the same values of ε. As a result of investigations structure shown in Fig. 5 was chosen which provides the worst boundary conditions for the considered LP.

An experiment has been made to find the significance of changes of maximum values of current density, depending on the lengths l_1 and l_2 larger than *l*.

Given that with decrease of length *l* impact of boundary conditions on LVCD increases, for experiment the value of $l = 3 \cdot r$ was chosen for it to be as small as possible (it is the smallest, because at $l = 2 \cdot r$ the interior edges are equal to zero (Fig. 5))

The value of *w* was selected equal to *l*. This value of *w* can be viewed as practically the worst, because with increase of *w* the impact of boundary conditions on LVCD increases with unacceptably large error ε. Experimental results do not depend on the value of *r*. Setting *r* to *1*, values $l=3$ and $w=3$ can be obtained. Due to position of branches values of l_1 and l_2 cannot exceed *l*. Thus, the value of one of them is fixed and

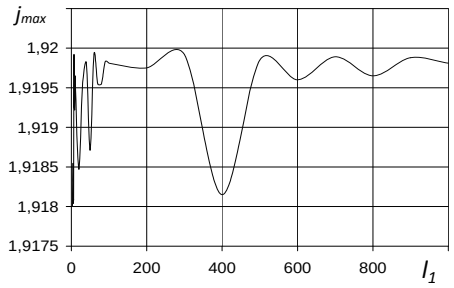

Fig. 6. Dependence of j_{max} on l_1, for $l_1 \geq l$.

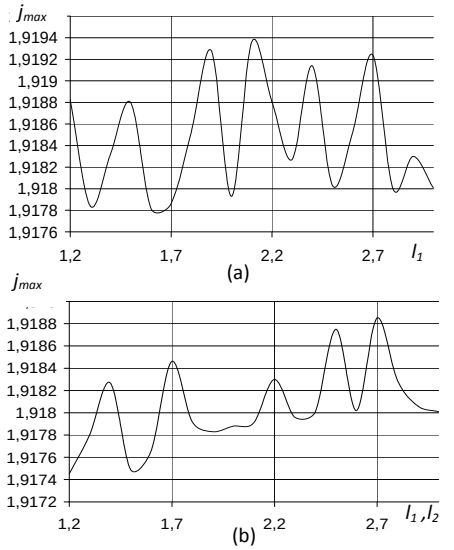

Fig. 7. Dependence of j_{max} a – on l_1, for $l_1 \leq l$, b – on l_1 and l_2 ($l_1 \leq l$, $l_2 \leq l$).

only the value of another changes. Based on the dependence of LVCD on l_1 obtained through the experiment, it can be concluded that for l_1 nearly equal to l a value of LVCD is obtained which is by no more than 1% less than LVCD for larger l_1 (Fig. 6).

To find dependence of LVCD on simultaneous change of l_1 and l_2, first l_1 was changed in the range less than l (Fig. 7a), then both l_1 and l_2 were changed (Fig. 7b). It can be stated that the LVCD values found for values larger than l will not change with increase of l_2. Values of l_1 and l_2 can be taken equal to l during calculation dependence of LVCD on model parameters.

In the result of experiments it was found that for the worst selected values ($l/w=1.5$), the relative difference of obtained LVCD values is *0.5…0.6%* compared to values obtained for values larger than l (Fig. 8).

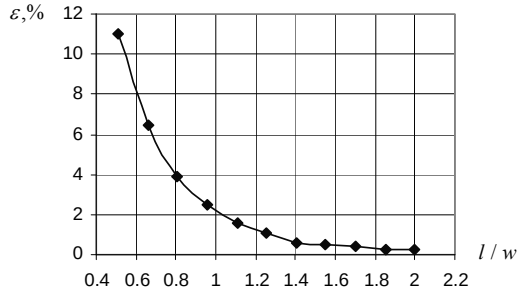

Fig. 8. Dependence of error ε on l/w.

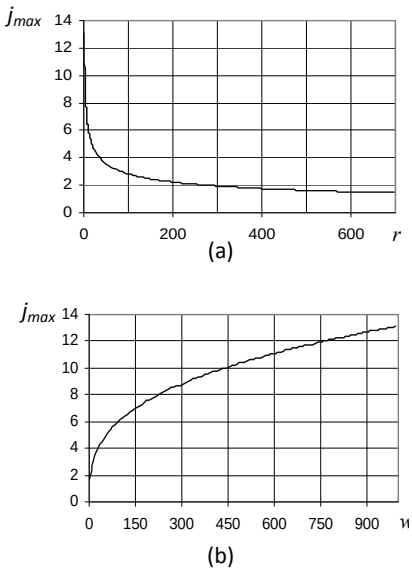

Fig. 9. Dependence of j_{max} on a – w, b – r

For considered LP, with the condition of $l/w \geq 1.5$ experiments were implemented to find the dependence of current density on parameters r and w. In the result it was obtained that j_{max} does not depend on w and r, thus it can be expressed as:

$$j_{max}=f(r)\cdot\varphi(w)\cdot j, \tag{2}$$

where

$$j=I/w \tag{3}$$

is the current density in uniform area. Thus it is the boundary condition for those edges of the considered LP, which have nonzero current flowing in the direction of normal.

To obtain functions f and φ two experiments were implemented resulting in dependencies of j_{max} on w (Fig. 9a) and r (Fig. 9b) with fixed value of another variable.

In the result of approximation of dependence function, the following was obtained for considered LP:

$$j_{max} = (13{,}2 \cdot r^{-0{,}33} - 0{,}06368) \cdot \tag{4}$$
$$\cdot (0{,}09743 \cdot w^{0{,}3365} + 0{,}0005986) \cdot j$$

Using expressions (2) and (3), for w this is obtained:

$$\frac{0{,}09743 \cdot w^{0{,}3365} + 0{,}0005986}{w} = \tag{5}$$
$$= \frac{j_{\max}}{I \cdot (13{,}2 \cdot r^{-0.33} - 0{,}06368)}$$

The general flow of developed method of current density verification is presented on Fig. 10.

TABLE II.
COMPUTER TIME AND MEMORY REQUIRED
TO OBTAIN THE CURRENT DENSITY DISTRIBUTION

Parameters	Circuit 1	Circuit 2	Circuit 3	Circuit4
Time, s	0.125	0.391	1.734	7.984
Memory, kB	1.3	8.7	28.9	97.4

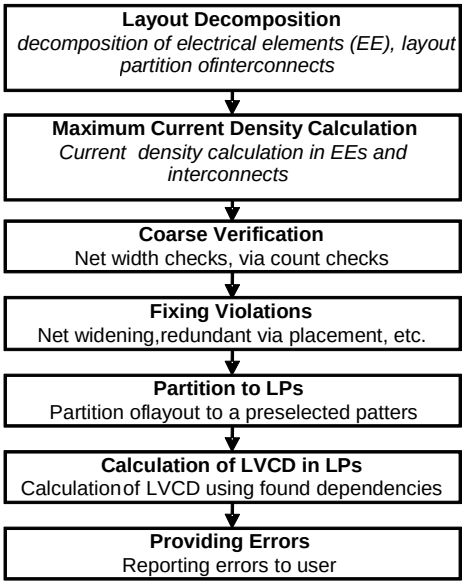

Fig. 10. General current density verification flow.

Experimental software implementing the proposed method was developed. Unlike industrial software, it does not need additional extraction and simulation steps. Experimental results obtained using software are shown in Table II. For a circuit with 50000 LPs, 104 minutes were required for calculation with conventional software, whereas with proposed method it took only ~10 minutes.

III. Conclusion

The developed method of current density verification in ICs and the experimental software package have indisputable advantages over existing similar tools and meet practical requirements of modern IC design.

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