Dynamics of Closed-loop ADC-NOT-DAC Circuits

Arthur E. Edang, Fredison A. Corminal, and Felicito S. Caluyo

***Abstract*—This article introduces a class of dynamical maps based on triadic circuits consisting of analog-to-digital converter (ADC), NOT gate/s, and a digital-to-analog converter (DAC). A NOT gate placed along one of the digital lines between the ADC and DAC produces a nonlinear transfer relationship. When the DAC's analog output is fed back as input to the ADC, the resulting closed-loop system exhibits a rich array of bifurcations leading to pseudo-randomness. Simulated results from a mathematical model match fairly well with those derived from an electronic circuit realization.**

***Index Terms*—Analog-to-digital converter, bifurcation, digital-to-analog converter, map, NOT gates.**

I. Introduction

ELECTRONICS and difference equations share a kind of affinity, especially in the study of nonlinear dynamics. This relationship is seen in circuit realizations of discrete-time systems such as those described by the logistic [1]–[9], tent [10]–[13], sine-circle [14]–[15], Henon [16]–[18], and Bernoulli [19]–[21] maps. These maps were first studied numerically, and it was usually after that that circuits were used to demonstrate and validate the results of mathematical predictions.

Conversely, there were circuits that existed long before engineers were able to present maps to describe them. An example is a thyristor circuit whose maximal values of anode-cathode voltages bifurcated as the frequency of the ac source was varied [22]. This led to the formulation of a first return map as a function of breakover voltage and ac frequency. Another is a discrete model reported by Chua and Lin [23] which arose from a second-order digital filter using 2's complement overflow nonlinearity in its accumulator. Then, there is a digital phase-locked loop whose nonlinearity is due to the combined effect of quantization and a sinusoidal phase detector [24]. Its output was observed to be periodic, quasi-periodic, and something more complex – all of which were later found to be consistent with the predictions of a novel difference equation. Underlying maps were also discovered in the operation of switching dc-dc power converters, particularly in the buck [25]–[26] and boost [27]–[28] regulators. Maps were likewise seen in low-pass and band-pass sigma-delta modulators [24].

Recently, it was reported in [29] that a family of maps arises from a closed-loop tandem of an analog-to-digital converter (ADC) and a nonlinearized digital-to-analog converter (NDAC). In that study, nonlinearity was observed after cutting one of the digital lines between the two converters, and tying it to logical *High* that severed input of the DAC. Other nonlinearities were created when additional lines were likewise altered, or instead tied to logical *Low*.

In this paper, the authors extended the membership of NDAC-based generators. The contribution is a class of triadic circuits consisting of an analog-to-digital converter (ADC), NOT gate, and a digital-to-analog converter (DAC). The presence of a logical inverter along one of the data lines from the ADC to the DAC results in a nonlinear relationship between the analog input and output signals of the two converters. Moreover, when the analog output is looped back to the input, it is observed that the circuit behaves as a map and generates a bifurcating sequence of bytes when a parameter is varied. More maps are found when other data lines are likewise altered, or NOT gates are simultaneously inserted in several lines. In that regard, this paper aims to report the results from investigations on sample members of this class of dynamical maps.

The rest of the paper is organized as follows: Section II presents the transfer curves of some of these new nonlinearities, their mathematical representations, and the numerically-derived bifurcation diagrams with respect to an identified system variable. In Section III, the details of the electronic circuit realization of one of these maps are discussed. The study is concluded in Section IV.

II. ADC-NOT-DAC Triad

In Fig. 1, one of $(2^n\text{-}1)$ ways to put NOT gates between n-bit converters is shown. As a means to distinguish one interposal from another, we introduce the following notation: for an 8-bit system, the positions of 'N' within a code indicate where the inverters are. For example, N111-1111 for Fig.1 means that an inverter was placed between the ADC's most significant bit (MSB) output and the corresponding MSB input of the DAC,

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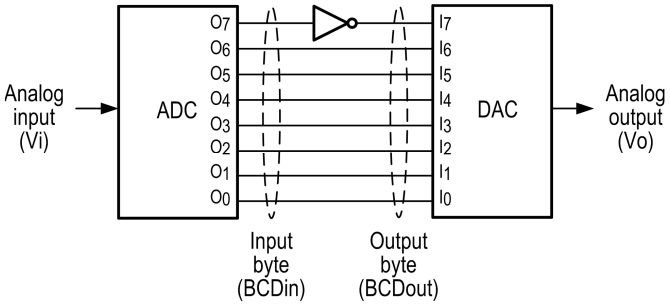

Fig. 1. ADC-NOT-DAC arrangement for producing a nonlinear transfer relationship.

while other data lines were left unchanged. In the following sections, three more configurations are presented: 1N11-1111, 1NN1-1111, and N1N1-1111.

A. Transfer Curve

The inclusion of the NOT gates forms several interesting input-output relationships. As depicted in each transfer curve of Fig. 2, *BCDin* stands for the ADC's binary-coded decimal (BCD) output, and *BCDout* refers to the DAC input. In the case of Fig. 2a, one may observe that whenever the MSB of *BCDin* is *Low*, *BCDout* exceeds *BCDin* by 2^7. Conversely, when MSB is *High*, BCDin is 2^7 units lower than *BCDout*. From these and a similar examination of Fig. 2b, the transfer function when there is a single inverter along the k^{th} data line may be generalized as

$$BCDout = \begin{cases} BCDin + 2^k & (I_k = 0) \\ BCDin - 2^k & (I_k = 1) \end{cases} \quad (1)$$

where I_k is the k^{th} bit of the input byte. Here, we assume that the least significant bit (LSB) is at line k=0. Then, with a slight modification, this expression can be likewise applied to Fig. 2c and Fig. 2d which have two inverters, one each along the k^{th} and j^{th} data lines, such that

$$BCDout = \begin{cases} BCDin + 2^j + 2^k & (I_j, I_k) = (0,0) \\ BCDin + 2^j - 2^k & (I_j, I_k) = (0,1) \\ BCDin - 2^j + 2^k & (I_j, I_k) = (1,0) \\ BCDin - 2^j - 2^k & (I_j, I_k) = (1,1) \end{cases} \quad (2)$$

B. Nonlinear Map

In each of the mentioned ADC-NOT-DAC triads, a map was produced when analog output (V_o) was looped back to the analog input (V_i). Taking into account discretization at the ADC input, the system can be modeled by considering the dynamics of *BCDout*. Assuming that *BCDout=g(BCDin)* as discussed in Section II-A, it can be shown that

$$BCDout_{m+1} = g\left(\left\lfloor (VREF / REF+) \times BCDout_m \right\rfloor\right) \quad (3)$$

where $\lfloor . \rfloor$ is the floor function, *VREF* and *REF+* are the reference voltages of the DAC and ADC, and *m* and *m+1* refer to the previous and present integer states of *BCDout*,

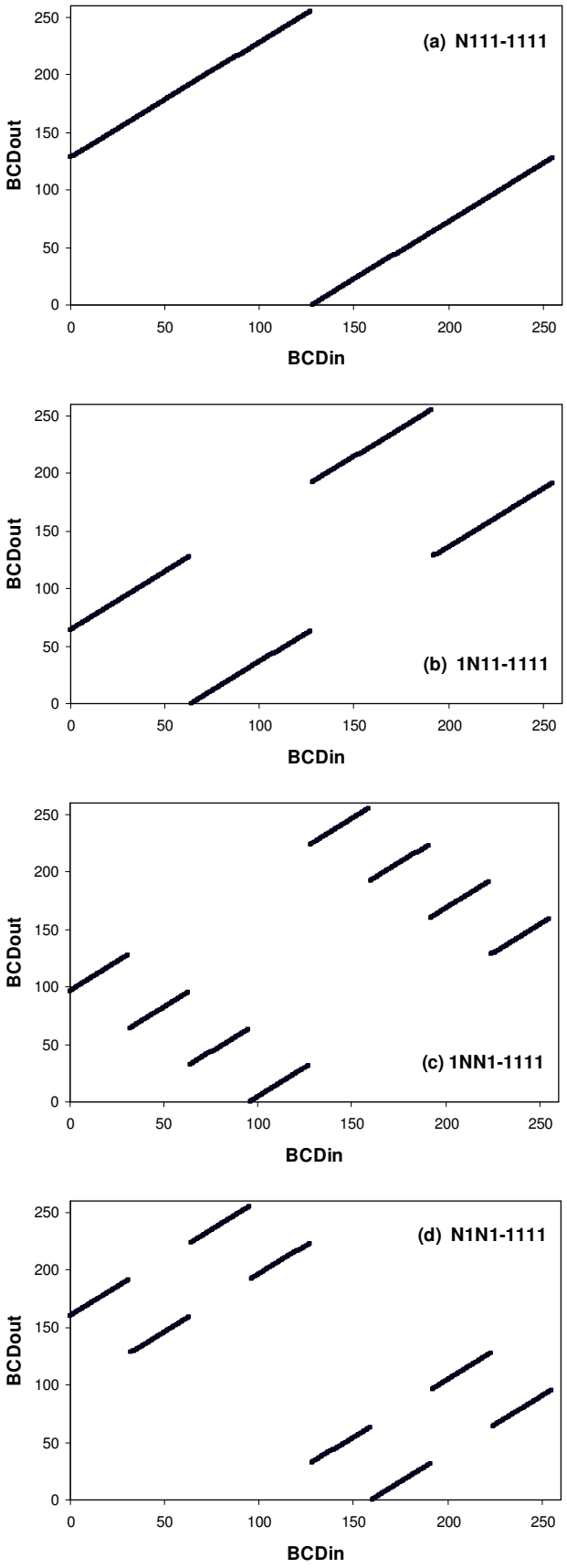

Fig. 2. Transfer curves for map (a) N111-1111, (b) 1N11-1111, (c) 1NN1-1111 and (d) N1N1-1111.

respectively. Note that (3) is identical to the map in [29] but now allows a larger membership for *g(.)*.

Numerical analysis showed that, for a fixed *REF+*, the maps exhibit many bifurcations as *VREF* was varied. For each map, we initially set *BCDout=g(0)* and *VREF=0*, ran the algorithm for 300 rounds to allow the transitory trajectories to die down, then recorded the ensuing 300 integer states of *BCDout*. This procedure was repeated for *VREF={0.02, 0.04, 0.06, …}* until it reached the point when the resulting *BCDout* sequence finally settled to a period-1 cycle. Results are depicted in Fig. 3. Alternatively, Fig. 4 shows the periodicity of *BCDout* for different *VREF* values.

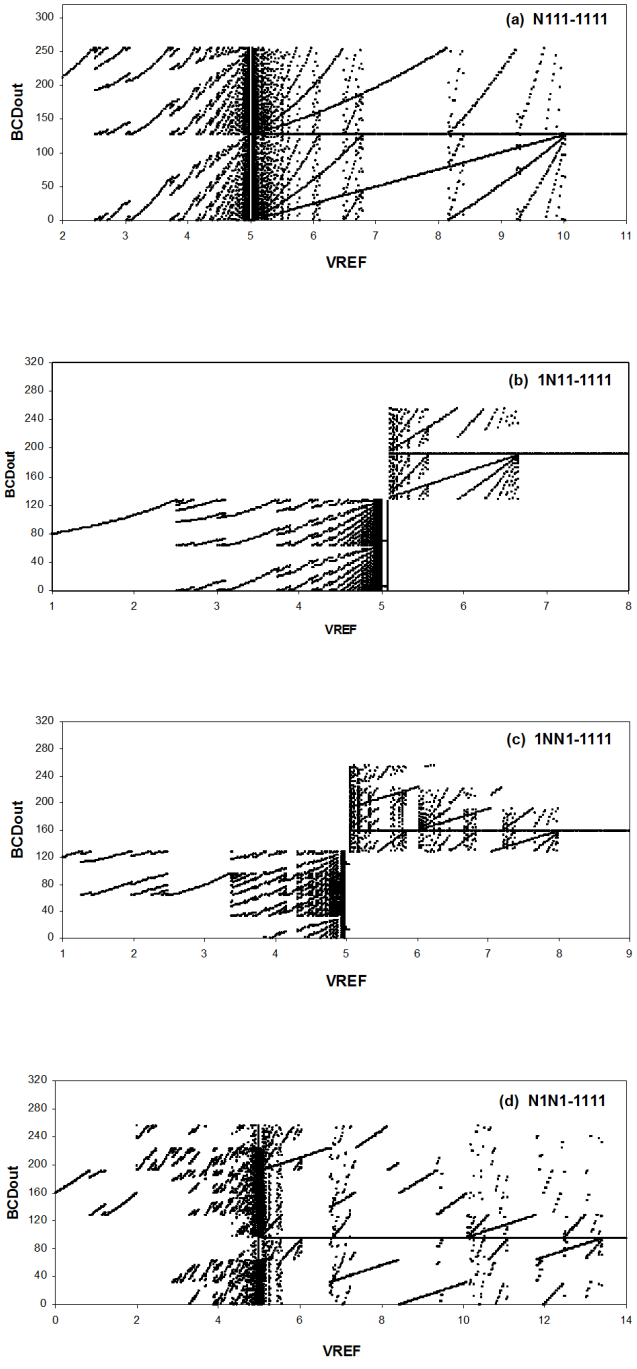

Fig. 3. Bifurcation diagrams for map (a) N111-1111, (b) 1N11-1111, (c) 1NN1-1111 and (d) N1N1-1111.

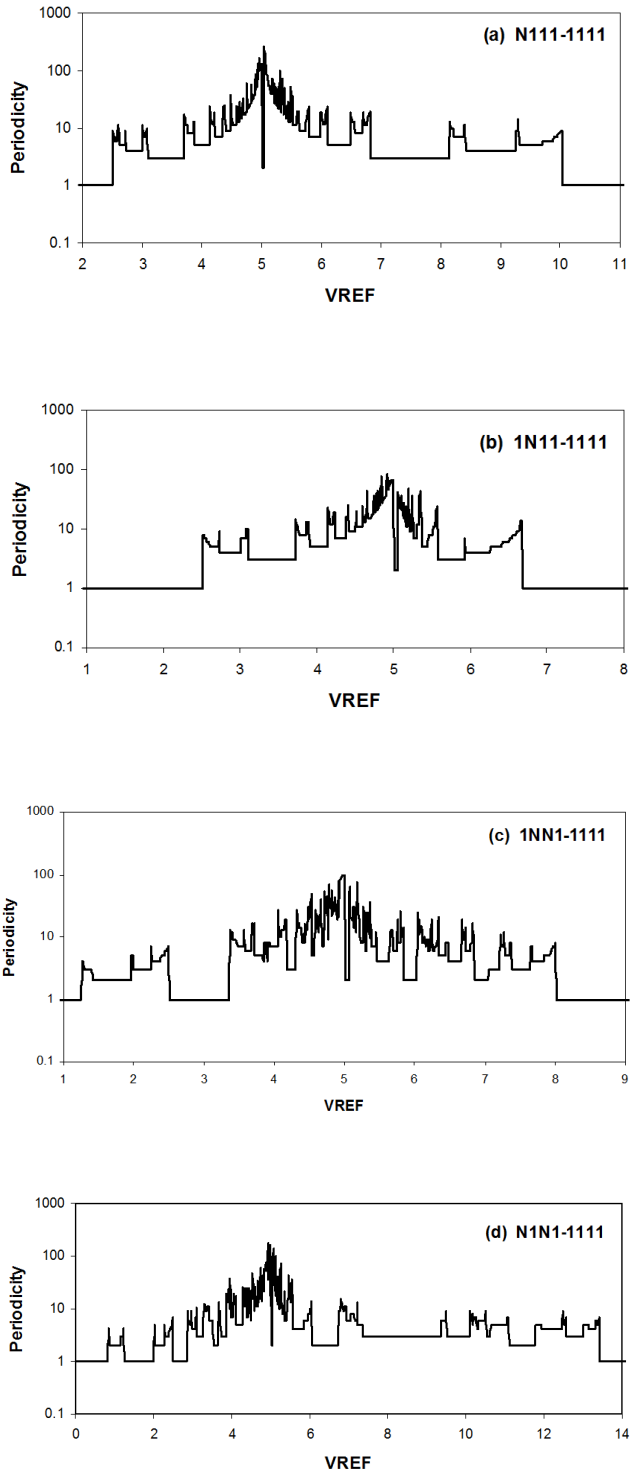

Fig. 4. The number of periodic BCD outputs per cycle as *VREF* is varied for map (a) N111-1111, (b) 1N11-1111, (c) 1NN1-1111 and (d) N1N1-1111. It was assumed that *REF+=5.00*.

For N111-1111 (Fig. 3a and Fig. 4a), a series of fixed points with increasing *BCDout* values precede the first periodic orbit

($P_{initial}$) which is a period-9 cycle at *VREF=2.51*. Within the range of 2.51 to 10.03, the map exhibits cycles whose periodicities (P) vary from $P_{min}=2$ at *VREF=5.01–5.03*, up to $P_{max}=251$ when *VREF=5.04*. That range ends with $P_{final}=9$ before the map bifurcates to a terminal fixed point at $BCDout_{final}=127$. These dynamical highlights together with those of the other ADC-NOT-DAC maps are summarized in Table 1.

TABLE I
DYNAMICAL HIGHLIGHTS OF ADC-NOT-DAC MAPS AT REF+=5.00

NDAC map	VREF range	$P_{initial}$	P_{final}	P_{min}	P_{max}	BCDout final
N111-1111	2.51-10.03	9	9	2	251	127
1N11-1111	2.52-6.67	8	14	2	84	191
1NN1-1111	1.26-8.01	4	8	1	97	159
N1N1-1111	0.84-13.42	4	7	1	174	95

III. ELECTRONIC CIRCUIT REALIZATION

Fig. 5 shows the electronic circuit implementation of the N111-1111 map. The core units consist of: (a) flash-type ADC (U1), (b) current-mode DAC (U4) [30], (c) NOT gate (U2c) between the converters, and (d) an octal D-type flip-flop (U3) for storing the results out of every iteration. Other details about the circuit and its operation are discussed in [29]. From the output (V_{o2}) of the auxiliary DAC (U5), the different bifurcations may be viewed when a sawtooth waveform is applied to the *VREF* of U4. Result is shown in Fig. 6.

While there is qualitative resemblance for most parts of the graphic when compared with Fig. 3a, one may observe a considerable disparity in the vicinity of *VREF=5.00*. In this region, there appear several fixed points whereas the numerical simulation shows only a period-2. The oscilloscope also showed that those points were wandering up and down without any discernable pattern.

A plausible explanation for this behavior is rooted in the transition of the map to higher *VREF*s. A finer numerical scan, in this case from *VREF=4.999* to *VREF=5.000*, reveals that each pair of period-2 states occurring at *VREF=5.000* corresponds to a particular *BCDout* found among the period-129 states of *VREF=4.999*. This relationship is shown in Fig. 7.

Considering that the sawtooth generator in Fig. 5 is not synchronized with the circuit's CLK signal, it can be argued that *BCDout* value at *VREF=4.999* just as *VREF* steps up to 5.000 volts is inconsistent; hence the ensuing period-2 states could be any of 129 pairs. It is likely that in every fresh cycle of the sawtooth, new period-2 states are filled. This results in the appearance of jerky bright spots on an analog oscilloscope and because visual persistence is inherent in scopes, one tends to see more than a pair of spots at any time.

It can be adduced that there is agreement between numerical and experimental results. Computer simulation shows the map's long-term behavior when its bifurcation parameter is repeatedly varied in a consistent manner. On the other hand, experimental results depict the map's response to a non-ideal bifurcation signal generator. Both asymptotic and transient states are exposed.

IV. CONCLUSION

We have introduced a new class of circuits based on ADC-NOT-DAC triads, which extends the membership of a previously reported nonlinear map. The circuit can find application in secure communications, particularly in data encryption and message authentication or hashing. The latter uses irreversible algorithms to generate unintelligible information out of a much larger message from the sender. Within hashing programs there are functions that employ

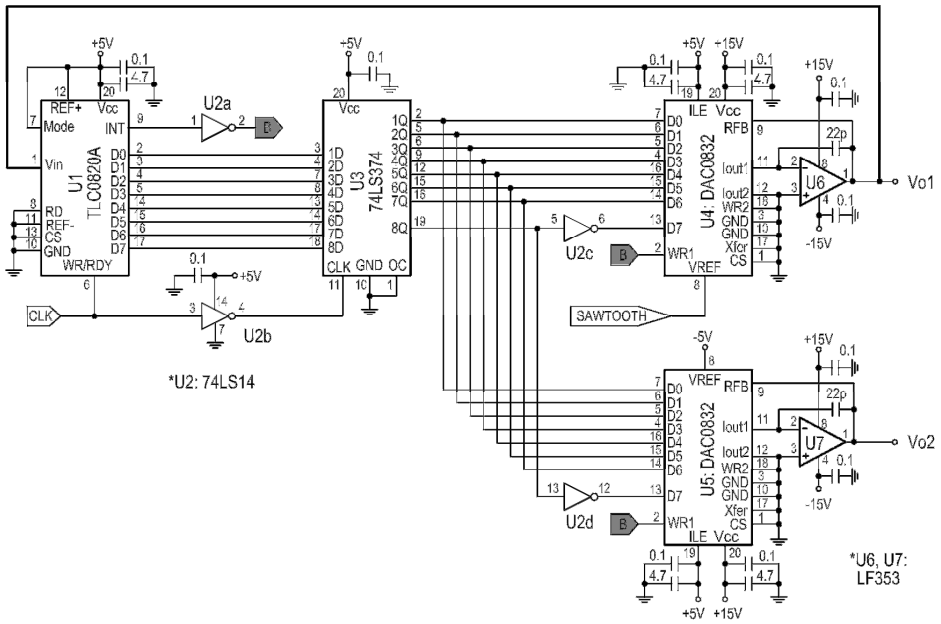

Fig. 5. Circuit realization for N111-1111 map.

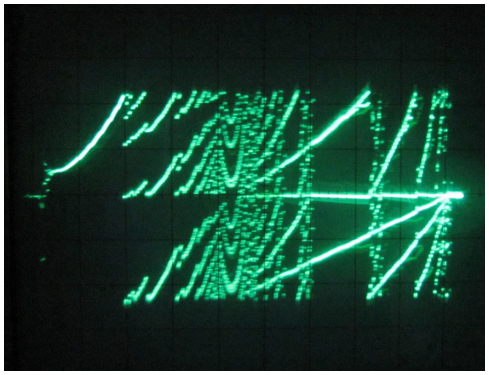

Fig. 6. Bifurcation plot for map N111-1111 circuit. Ch.1 (0.1V/div) at U4's VREF; Ch.2 (0.1V/div) at V_{o2}.

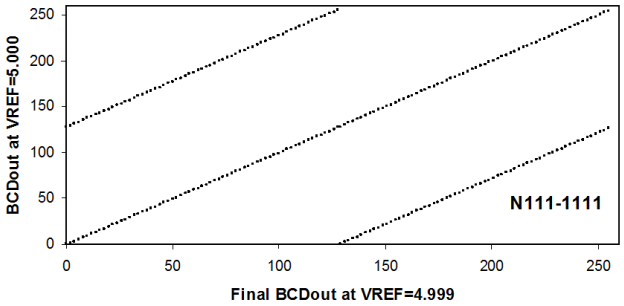

Fig. 7. Relationship between the terminal *BCDout* state at *VREF=4.999* and the ensuing period-2 states at *VREF=5.000* for map N111-1111.

modulo addition and subtraction, exclusive-OR, bit-swapping and bit-rotation, and randomized initializations. With this collection, the first author is investigating the utility of NDAC-based sequences in constructions for hash functions.

In contrast with popular maps that are built out of analog devices, the triadic NDAC map is predominantly digital. This feature makes interfacing easier, and frees the microprocessor from the task of generating pseudo-random sequences for cryptographic encryption. Furthermore, the adjustable *VREF* augurs the possibility of a secure system similar to frequency-hopping spread spectrum. This is a target area of forthcoming investigations.

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