Improved PLL for Power Generation Systems Operating under Real Grid Conditions

Evgenije M. Adžić, Milan S. Adžić, and Vladimir A. Katić

***Abstract*—Distributed power generation systems (DPGS) based on renewable energy sources need accurate grid phase angle information in order to achieve different control algorithms usual for this application. Phase-locked loop (PLL) is the most modern and most common method for determination of the phase angle and frequency of the grid voltage. However, there are still serious limitations of reported PLL algorithms in real grid voltage conditions, as in unbalanced and distorted distribution grid. This paper proposes improved PLL which gives excellent and almost perfect grid voltage phase angle and frequency in highly unbalanced and distorted grid. This is achieved by a cascade of finite impulse response filters which eliminates characteristic harmonic components and extracts only fundamental harmonic signal. In that way, proposed PLL allows setting of higher bandwidth frequency of the PLL filter and much faster response which is especially important during grid voltage sags and frequency variations. Performance has been evaluated in details through simulation in Matlab/Simulink.**

***Index Terms*—Distributed power generation systems, synchronization method, phase-locked loop, distorted grid.**

I. Introduction

THE worldwide electrical energy consumption is rising. Therefore, increase of the demands on the power capacities, efficient generation, distribution and utilization of energy are noticeable [1]. In power systems sector there is a key movement from a relatively small number of large, centrally controlled conventional power stations connected to the transmission system towards a greater number renewable energy generating plants such as wind turbines, photovoltaic generators and fuel cells, now connected to the distribution grid. Power electronics, being the technology for efficiently converting electrical power, represents essential part that enabled such a development. Power electronics devices serve as an interface between DPGS and a grid, with the task to adapt the produced power to the numerous grid requirements.

In general, DPGS contains a power converter connected to the grid, whose main task is to control the transfer of active and reactive power between the DPGS and the grid. Different control structures for the grid connected converter have been proposed in the relevant literature [2], where grid voltage oriented vector control is usually employed [3]. Vector control principle depends on accurate and precise determination of the grid voltage phase angle, which is required in order to achieve independent control of active and reactive power. This task is performed by grid synchronization unit.

The quality of the grid synchronization, in addition to current regulators in the control structure, is a key factor which determines the quality of the entire control structure [2], [4]. Error in the phase angle estimation can lead to significant error in the imposed converter output voltage and its distortion, thus resulting in the error between the reference and injected power into the grid and in inappropriate operation during various grid disturbances.

In the literature related to the grid synchronization field, different methods can be found which are applied in practice for DPGS [2], [4]. The zero crossing detection is the simplest method, but achieve slow dynamic and a fast tracking of the phase angle is impossible. This method is subject to a great influence of grid voltage harmonics and voltage dips. There are methods based on filtering of grid voltage in α-β stationary and rotating d-q reference frame, although filtering enters delay in the output phase angle signal which makes this method vulnerable to a relatively frequent voltage sags in the distribution grid. The most common method used today for grid synchronization is a phase-locked loop (PLL) implemented in the d-q synchronous rotating reference frame, which block diagram is shown in Fig.1. It contains a filter, usually proportional-integral (PI) controller type, that determines its dynamics. Especially, it is influenced by presence of unbalance and distortion in the grid voltage. Therefore, filter bandwidth is a compromise between filtering undesirable harmonics that occur in the PLL system due to the voltage unbalance and harmonics, and fast response time necessary for tracking voltage during a voltage sags and frequency variations in the grid. Therefore, it is often necessary to significantly reduce the filter bandwidth at the expense of poor and slow response during the grid disturbances.

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E. M. Adzic is with the Faculty of Technical Sciences, University of Novi Sad, Trg Dositeja Obradovica 6, Novi Sad, Serbia (phone: +381214852504; fax: +381214750572; e-mail: evgenije@ uns.ac.rs).

M. S. Adzic is with the Subotica Tech – College of Applied Sciences, University of Novi Sad, Marka Oreskovica 16, Subotica, Serbia (e-mail: adzicm@vts.su.ac.rs).

V. A. Katic is with the Faculty of Technical Sciences, University of Novi Sad, Serbia (e-mail: katav@uns.ac.rs).

In this paper, an improved pre-filter based PLL for three-phase grid interface converters is proposed. Proposed PLL obtains accurate and almost perfect grid voltage phase angle and frequency even in highly unbalanced and distorted voltage conditions. This is achieved by employing a cascade of finite impulse response filters (FIR) which eliminates characteristic harmonic components in the PLL system caused by grid voltage distortions and extracts only fundamental harmonic signal represented in d-q reference frame. With proposed PLL it is possible to have fast dynamic and consequently it has much better response with grid frequency variations and voltage sags. Extensive simulation results are provided for validation of the proposed algorithm.

II. PLL Principle of Operation and Model

A block diagram of the conventional PLL implemented in d-q synchronous rotating reference frame is depicted in Fig. 1. Its principle of operation can be explained through the following steps:

• Three-phase grid voltages v_a, v_b, and v_c are measured. At first, a balanced three-phase set of voltages could be assumed, where θ represent actual phase angle of grid voltage in the first phase (a):

$$\begin{aligned} v_a &= V_g \cdot \cos\theta \\ v_b &= V_g \cdot \cos(\theta - 2\pi/3) \\ v_c &= V_g \cdot \cos(\theta + 2\pi/3) \end{aligned} \tag{1}$$

• Measured phase voltages are transformed to a α-β stationary reference frame using Clarke transformation, resulting in voltage components v_α and v_β:

$$\begin{aligned} v_\alpha &= 2/3 \cdot [v_a - (v_b - v_c)/2] \\ v_\beta &= 1/\sqrt{3} \cdot (v_b - v_c) \end{aligned} \tag{2}$$

• α-β voltage components are transformed to d-q synchronous rotating reference frame using Park transformation with estimated phase angle $\hat{\theta}$ from the PLL output. Grid voltage components v_d and v_q are obtained:

$$\begin{aligned} v_d &= v_\alpha \cdot \cos\hat{\theta} + v_\beta \cdot \sin\hat{\theta} \\ v_q &= -v_\alpha \cdot \sin\hat{\theta} + v_\beta \cdot \cos\hat{\theta} \end{aligned} \tag{3}$$

After applying Park transformation d-q components are equal to:

$$\begin{aligned} v_q &= V_g \cdot \sin(\theta - \hat{\theta}) \\ v_d &= V_g \cdot \cos(\theta - \hat{\theta}) \end{aligned} \tag{4}$$

• Error signal e is formed by subtracting the reference signal v_q^* and obtained grid voltage component v_q, which is set to the input of PLL filter. Setting the reference v_q^* to 0 is responsible for tracking the phase angle of grid phase voltage (v_a). As PLL filter, proportional-integral (PI) controller is selected, in order to reduce the error signal e to zero:

$$e = 0 - v_q = -V_g \cdot \sin(\theta - \hat{\theta}) \;\wedge\; e = 0 \quad \Rightarrow \quad \hat{\theta} = \theta \tag{5}$$

which would lead to steady-state equalization of estimated and actual grid voltage phase angle. PI controller is selected as the filter type, because in the steady-state the error signal would be zero for abrupt changes in the voltage phase angle, but also for the abrupt changes of the voltage frequency (ramp input), which is expected in DPGS applications due to a weak distribution grid where failures are common. Near the steady-state, where small difference between the real and estimated phase angle exist, error signal can be linearized in order to obtain a suitable model and simplify PLL analysis:

$$e \approx V_g \cdot (\theta - \hat{\theta}) \tag{6}$$

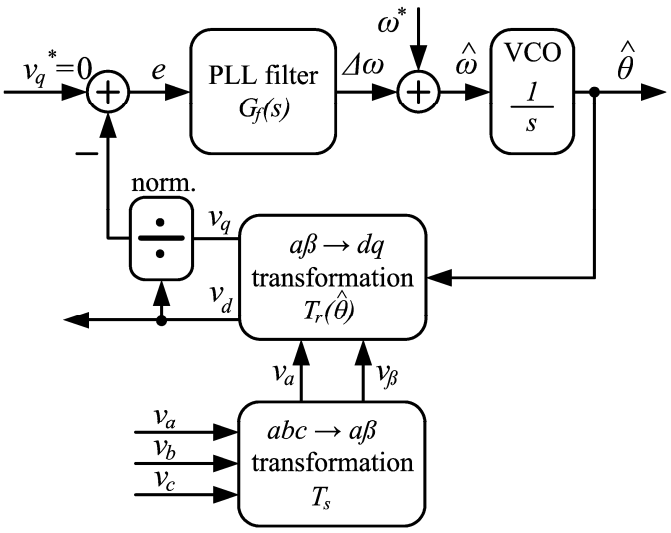

Fig. 1. Block diagram of the conventional dq-PLL system.

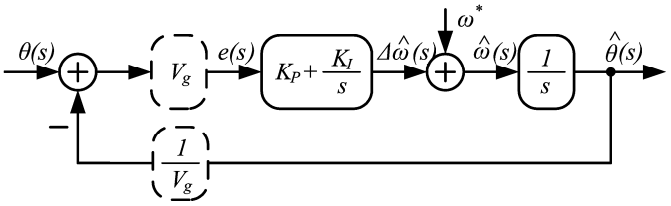

Fig. 2. Linearized model of conventional d-q PLL system.

• Base on error signal e, PI controller calculates the grid voltage angular frequency change $\Delta\omega$, which in the continuous Laplace s-domain can be represented with:

$$\Delta\omega(s) = G_f(s) \cdot e(s) = \left(K_P + \frac{K_I}{s}\right) \cdot e(s) \tag{7}$$

• $\Delta\omega$ at the PI controller output is added to the reference angular frequency ω^*, which is set to the value of actual grid angular frequency (e.g. $2\pi \cdot 50$ rad/s). This would result with a estimated grid angular frequency $\hat{\omega}$ value .

• Integrating the estimated angular frequency $\hat{\omega}$ in time, estimated grid voltage phase angle is obtained:

$$\hat{\theta}(s) = \frac{1}{s} \cdot \hat{\omega}(s) \tag{8}$$

• Estimated phase angle $\hat{\theta}$ is used to calculate new voltage d-q components, until v_q becomes zero and v_d becomes constant equal to the grid voltage amplitude, and finally when the difference between actual phase angle of the grid voltage and estimated phase angle becomes zero.

• Estimated grid voltage amplitude (v_d) is used to

normalize voltage q-component at the PI controller feedback input, in order to eliminate grid voltage amplitude variations influence on the PLL response [9] determined and designed with filter (PI) parameters (see Fig. 2).

From previous, linearized PLL model in continuous Laplace domain could be extracted, which is shown in Fig. 2. The transfer function of the closed loop conventional d-q PLL is of second order with one zero and could be rewritten in general form as:

$$G_c(s) = \frac{s \cdot K_P + K_I}{s^2 + s \cdot K_P + K_I} = \frac{s \cdot 2\xi\omega_n + \omega_n^2}{s^2 + s \cdot 2\xi\omega_n + \omega_n^2} \tag{9}$$

where are: ξ – relative damping factor, and ω_n – system natural frequency. It is the size of ξ and ω_n which characterize system performance in the transient-state in time domain. From the transfer function form, one could conclude that the desired character of the PLL response is achieved by tuning parameters of the PI controller [8]:

$$\omega_n = \sqrt{K_I} \quad \xi = \frac{K_P}{2}\sqrt{\frac{1}{K_I}} \quad K_I = \frac{K_P}{T_I} \tag{10}$$

III. PLL in Unbalanced and Distorted Grid Conditions

In practice, distribution grid voltage has not a pure sinusoidal waveform but it is disturbed by various factors such as load unbalance and nonlinearities [5]. Resulted three-phase voltage waveforms are unbalanced and with harmonics. The possible grid voltage signal offset is often introduced by the measurement and conversion electronic circuits, but its influence is not considered in this paper.

A. Grid Voltage Unbalance

The unbalanced set of three-phase voltages can be expressed as:

$$\begin{aligned} v_a &= V_g \cdot \cos\theta \\ v_b &= V_g \cdot (1+a) \cdot \cos(\theta - 2\pi/3) \\ v_c &= V_g \cdot (1+b) \cdot \cos(\theta + 2\pi/3) \end{aligned} \tag{11}$$

where constants a and b indicates unbalance level. After transformation in α-β stationary reference frame they can be expressed as:

$$\begin{aligned} v_\alpha &= V_g \cdot \cos\theta + V_g \cdot \frac{a+b}{6} \cdot \cos\theta + V_g \cdot \frac{b-a}{2\sqrt{3}} \cdot \sin\theta \\ v_\beta &= V_g \cdot \sin\theta + V_g \cdot \frac{a+b}{2} \cdot \sin\theta + V_g \cdot \frac{b-a}{2\sqrt{3}} \cdot \cos\theta \end{aligned} \tag{12}$$

The second and third terms in (12) are produced by the phase unbalance. Assuming that error $e = \theta - \hat{\theta}$ is small (near zero in steady-state) and $\theta + \hat{\theta} = 2\theta$, the voltage d-q components can be derived after Park transform as:

$$\begin{aligned} v_d &= V_g + V_g \cdot \frac{a+b}{3} + V_g \cdot \left(\frac{b-a}{2\sqrt{3}} \cdot \sin 2\theta - \frac{a+b}{6} \cdot \cos 2\theta \right) \\ v_q &= V_g \cdot \sin e + V_g \cdot \frac{a+b}{3} \cdot \sin e \\ &+ V_g \cdot \left(\frac{a+b}{6} \cdot \sin 2\theta + \frac{b-a}{2\sqrt{3}} \cdot \cos 2\theta \right) \end{aligned} \tag{13}$$

Since the voltage q-component is controlled to zero by the PLL system, error caused by unbalanced grid would be:

$$e \approx -V_g \cdot \left(\frac{a+b}{6} \cdot \sin 2\theta + \frac{b-a}{2\sqrt{3}} \cdot \cos 2\theta \right) \tag{14}$$

One can note that second harmonic component would propagate through the PLL system if three-phase grid voltage is unbalanced.

B. Grid Voltage Harmonics

Another significant effect which influences PLL operation is voltage harmonics. A consequence of numerous nonlinear loads in the distribution grid is distorted grid voltage waveform, which is usually flattened (or sharpened at the converter-side of the distribution transformer) in the region of its maximal values, and contains dominant 5th and 7th harmonic components. Therefore, distribution grid voltage with the dominant harmonics can be represented as follows:

$$\begin{aligned} v_a &= V_g \cdot \cos\theta + V_{g5} \cdot \cos 5\theta + V_{g7} \cdot \cos 7\theta \\ v_b &= V_g \cdot \cos(\theta - 2\pi/3) + V_{g5} \cdot \cos[5 \cdot (\theta - 2\pi/3)] + \\ &+ V_{g7} \cdot \cos[7 \cdot (\theta - 2\pi/3)] \\ v_c &= V_g \cdot \cos(\theta + 2\pi/3) + V_{g5} \cdot \cos[5 \cdot (\theta + 2\pi/3)] + \\ &+ V_{g7} \cdot \cos[7 \cdot (\theta + 2\pi/3)] \end{aligned} \tag{15}$$

where V_{g5} and V_{g7} represents amplitudes of 5th and 7th harmonics, respectively. α-β stationary reference frame components of the grid voltage given with (15) can be expressed as:

$$\begin{aligned} v_\alpha &= V_g \cdot \cos\theta + V_{g5} \cdot \cos 5\theta + V_{g7} \cdot \cos 7\theta \\ v_\beta &= V_g \cdot \sin\theta - V_{g5} \cdot \sin 5\theta + V_{g7} \cdot \sin 7\theta \end{aligned} \tag{16}$$

The second and third terms in (16) are produced by the voltage harmonics. Assuming that error $e = \theta - \hat{\theta}$ is small (near zero in steady-state) and $5\theta + \hat{\theta} = 6\theta$ and $7\theta - \hat{\theta} = 6\theta$, the voltage d-q components can be derived after Park transformation as:

$$\begin{aligned} v_d &= V_g + (V_{g5} + V_{g7}) \cdot \cos 6\theta \\ v_q &= V_g \cdot \sin e - (V_{g5} - V_{g7}) \cdot \sin 6\theta \end{aligned} \tag{17}$$

Therefore, the PLL error which would occur in estimated phase angle and frequency due to the 5th and 7th harmonic can be represented with following expression:

$$e \approx (V_{g5} - V_{g7}) \cdot \sin 6\theta \tag{18}$$

Besides the sixth harmonic component in the PLL system, frequency components of 12θ, 18θ, ... would appear if higher harmonic components, characteristic for the distribution grid, are included. They are not considered in this paper, because

they are negligibly small in real grid compared to 5th and 7th harmonics.

IV. Criteria and Selection of PLL Filter Parameters

PLL operation is subject to the influence of various disturbances in the grid, as shown in previous section. Grid voltages unbalance and distortion introduce second and (dominantly) sixth harmonic components (errors) in d-q PLL system.

In addition, in section II it is shown that the PLL system dynamic depends on the parameters of the filter. It can be concluded that the slow dynamic of the filter would give very filtered and stable phase angle, but with longer synchronization time. On the other hand, filter with high dynamic would give a phase angle that follows rapid variations in a grid voltage (necessary during grid faults), but the grid disturbances (harmonics, unbalance, offset) would propagate through the filter, resulting in erroneous phase angle. Therefore, when designing a PLL filter, one usually must make a compromise, or select slow or fast filter dynamic due to the purpose of the system.

Most commonly in relevant literature, one can found that cut-off frequency of 50 Hz or response settling time of 20 ms are selected for PLL filter (if grid frequency is 50 Hz), explaining it with the fact that grid frequency needs to be fast followed [2]. It is the right selection if synchronization algorithm is employed to detect or response to grid faults and frequency variations. However, undesirable consequence is that a large bandwidth (due to the high filter gains) amplifies and propagates even small harmonics due to the grid voltage distortion. It represents large disadvantage for synchronizing the control variables to the grid voltage vector in order to have an accurate synchronization and good quality control. Considering that grid regulations in some countries require normal operation of distributed generators in the case of grid frequencies between 47 and 53 Hz, another selection of cut-off frequency could be around 3 Hz. Such PLL synchronization system would have opposite behavior compare to previous one (where cut-off frequency is 50 Hz).

It is known that in the general case of a second order system step response, there are two parameters defined: settling time T_{set}, and overshoot P, that determines system performance in the transient-state in time-domain. Their correlation with relative damping factor ξ, and system natural frequency ω_n, could be expressed with following:

$$\xi = \sqrt{\frac{(\ln P/\pi)^2}{1+(\ln P/\pi)^2}} \qquad \omega_n = \frac{4{,}6}{\xi \cdot T_{set}} \tag{19}$$

where T_{set} represents required time for response signal to enter in ±1% zone around steady-state reference step value. Correlations (10) and (19) provide, based on pre-specified settling time T_{set} and overshoot P, determination of the required gains in PLL filter. Another approach for filter design is to use desired system frequency bandwidth ω_{bw} instead of setlling time, as an input design parameter. In a rough approximation for second-order system one can use equal bandwidth and system natural frequelncy, or could use following exact correlation:

$$\omega_{bw} = \omega_n \cdot \sqrt{\left|2\xi^2 - 1\right| + \sqrt{\left|\xi^4 - 4\xi^2 + 2\right|}} \tag{20}$$

It is desirable that the PLL response has no excessive overshoot and no oscillations in order to avoid posible active and reactive power oscillations between a grid-side converter of distributed generators and a grid [4]. It is considered that the response with overshoot less than 5% is well-damped, so the damping coefficient ξ should be larger than 0.7. For desired aperiodical response ξ = 1, and based on given equations, parameters of the PLL filter are supposed to be as follows:

$$K_P = \sqrt{2} \cdot \omega_{bw} \quad \wedge \quad K_I = \frac{\omega_{bw}^2}{2} \left(K_I^z = K_I T_s\right) \tag{21}$$

For example, for bandwidth frequency f_{bw} = 3 Hz parameters K_P = 26.6 and K_I = 177.6 are obtained. The digital filter implementation (discrete z-domain) integral gain should be multiplied by the PLL loop sampling period T_s. Figs 3 and 4 gives step time-response and frequency response for design bandwidths of 3 Hz and 50 Hz, respectively. From Fig. 3 it can be observed that in both cases response overshoot is larger then designed and equal to 13.5 %. Fig. 4 shows slightly deviation of achieved bandwidths 5.2 Hz and 87.5 Hz compare to 3 Hz and 50 Hz set by design. These variations are consequences of existence of zero in the PLL transfer function that has been ignored during design. In order to eliminate this effect, some authors suggest introducing a lead-lag compensator in the PLL loop [2].

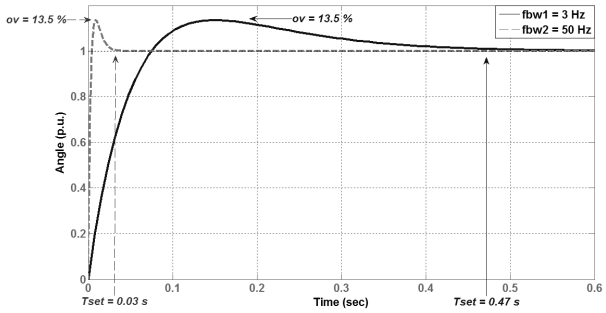

Fig. 3. Conventional d-q PLL step response for two different filter desired frequency bandwidth – 3 Hz (solid line) and 50 Hz (dashed line).

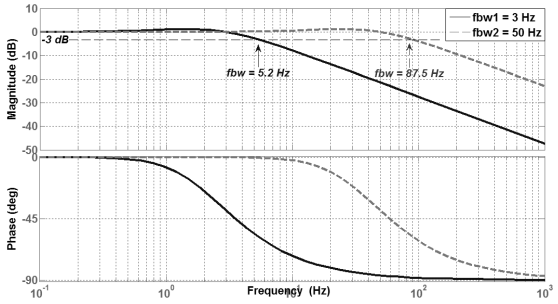

Fig. 4. Conventional d-q PLL frequency response for two different filter desired frequency bandwidth – 3 Hz (solid line) and 50 Hz (dashed line).

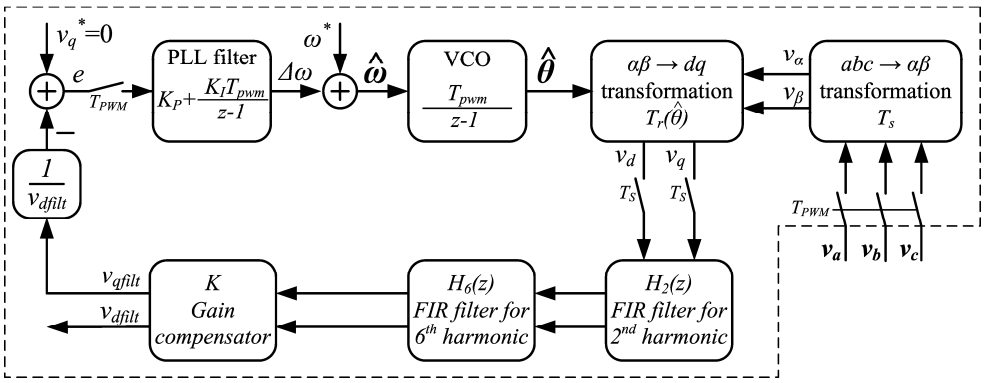

Fig. 5. Block diagram of the proposed pre-filter based d-q PLL system. Pre-filtering done on d-q voltage components eliminates characteristic harmonics influence.

V. PROPOSED PLL WITH PRE-FILTERING

In this section, an improved pre-filter based PLL is described and analyzed in details, which is simultaneously capable for rejecting characteristic errors due to grid unbalance and distortion and for achieving fast and appropriate response during grid frequency variations and voltage sags.

Proposed method basically consists of a synthesis of the second order FIR subsections that eliminates characteristic harmonic components which could occur in the PLL estimated phase angle and frequency. The complete FIR filter is implemented as a cascade of these modules. Block diagram of the proposed PLL is depicted in Fig. 5. It can be observed that pre-filters are used for rejecting harmonics in voltage d-q components and then used as inputs for conventional PLL. All further analysis and simulations are done in discrete z-domain.

Second order FIR filter which eliminates harmonic component f_i and have unity gain for selected fundamental frequency f_1 can be expressed as:

$$H_i(z)=\frac{1-2\cos(2\pi f_i/f_s)z^{-1}+z^{-2}}{2\left|\cos(2\pi f_1/f_s)-\cos(i\cdot 2\pi f_1/f_s)\right|} \qquad (22)$$

where i represent harmonic order for which transfer function have zero gain. In discrete domain term z^{-1} represent sample in previous sampling period, where f_s is the sampling frequency. In Fig. 5, $H_2(z)$ denotes transfer function of FIR filter employed to remove second harmonic component in PLL due to unbalanced grid, and $H_6(z)$ denotes FIR transfer function dedicated for removing sixth harmonic component due to distorted grid with 5^{th} and 7^{th} harmonics.

Amplitude- and phase-frequency characteristic of the FIR filters cascade is denoted in Fig. 6. One can observe that the filter completely attenuates characteristic harmonics and it has unity-gain for grid frequency (50 Hz). Good feature of the proposed filter is that it does not introduce delay for constant signal such are d-q components. That means there is neither need for phase compensator, as in [6], which would correct introduced phase shift by filters (at fundamental frequency) if it was implemented in original phase abc-domain. However, gain correction is needed and from given Bode diagram in Fig. 6 one can found that correction gain is equal to K = 1/1.4142 (=1/√2).

Special consideration must be taken into account when choosing sampling frequency for FIR filters [11]. On the one hand, it is desirable to have as highest possible sampling frequency (e.g. at pulse-width modulation level in power converters) in order to have fast updating of estimated phase angle and small error due to discretization. This is especially important in the case when FIR filtering is done in original phase abc-domain, but not the case when it is done in synchronous rotating reference frame where d-q components are constant values in steady-state. On the second hand, FIR filter (and also phase compensator) has amplitude characteristic with an increasing gain for higher frequencies then zero-gain frequency f_i, which is denoted in Fig. 7. Between designed zero-gain frequency f_i = 300Hz and half of sampling frequency $f_s/2$ = 4000/2 Hz, such filter would significantly amplify eventual higher harmonics occurring in

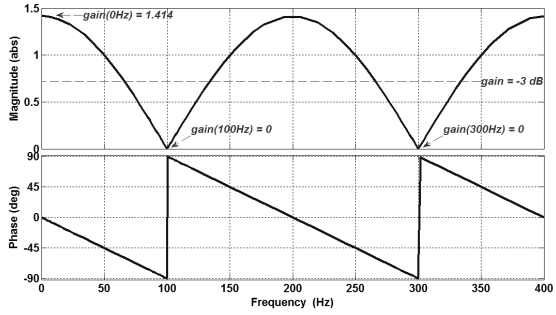

Fig. 6. Frequency characteristic of FIR filters cascade.

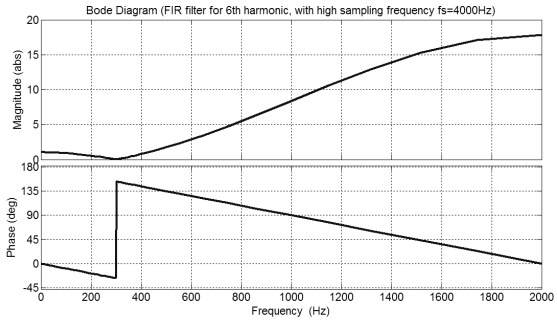

Fig. 7. Example of FIR filter frequency characteristic with high sampling frequency (fs = 4 kHz). High gains for higher frequencies are not acceptable.

the system. Considering the existence of other higher harmonics in the grid (11^{th}, 13^{th}...) as well as the presence of a significant noise typical for this application, previous fact put limitations for selecting sampling frequency f_s. That is the reason why in this paper sampling frequency is chosen to be equal to 800 Hz. In that way proposed FIR filter does not propagate next possible 12^{th} harmonic through the PLL system, due to 11^{th} and 13^{th} harmonic components in the grid voltage.

Fig. 8 shows frequency response of entire proposed PLL structure with FIR pre-filtering. Bandwidth frequency used in (conventional) PLL filter design is 25 Hz. Fig. 8 validates that proposed PLL has high frequency bandwidth (62.3 Hz) and as a consequence fast response required for tracking grid voltage angle during grid faults, but simultaneously cancels characteristic harmonic components at 100 Hz and 300 Hz. Gain for constant signals equals to 3 dB (√2 abs.) indicating that gain compensator (1/√2) must be used (look Fig. 5).

VI. Simulation Results

In this section, simulation results which verify effectiveness and usefulness of the proposed PLL algorithm are presented. Simulation is carried out in MATLAB/Simulink. During course of this work at the input of the simulated PLL system there was a highly distorted and unbalanced grid voltage with nominal grid frequency of 50 Hz.

Fig. 9 shows grid voltage waveforms used in the simulation. Fundamental harmonic with amplitude 1.0 p.u. is distorted with 5^{th} and 7^{th} harmonics, each with amplitude 0.05 p.u. In that way, total harmonic distortion (THD) of the simulated grid voltage is 7.07% which is higher then allowed by standards (5%) for the distribution grid. Phase shift of the harmonics is set in order to have typical waveform of the grid voltage at which power converter is connected. Unbalance of 10% is additionally introduced in the voltage waveforms, with constants indicating unbalance level a= -0.1 and b = 0.1.

At first, the proposed synchronization algorithm is tested against phase angle jumps and response was compared to conventional PLL. Change in reference q-voltage component at the PLL input is analogue to the grid voltage phase jump, but response details are easier to observe and analyze. Obtained response details are important because they would determine system response during faults where grid voltage could experience phase jump [10]. Voltage amplitude change during faults would result is second harmonic content in PLL system, so it is in some extent included by introduced unbalance (10%). Figs 10 and 11 illustrates behavior of conventional and proposed PLL in the situation of highly disturbed grid voltages (from Fig. 9) when q-voltage reference is set to 0 at 0.04 s (equivalent phase jump 90^0) and to 0.5 p.u. at instant 0.6 s (equivalent phase jump of 60^0). As it can be observed, the proposed PLL is able to track the new phase angle in about 2 fundamental periods (0.04 s), with a 20 % overshoot during transient. This is due to the higher bandwidth 25 Hz set in proposed system, compare to 3 Hz in conventional PLL which is set in order to limit d-q voltage components oscillations due to the unbalanced and distorted grid. Even though, oscillations in conventional system are much larger, and it could be observed in Fig. 12. It gives q-voltage component during 2 fundamental voltage periods, in

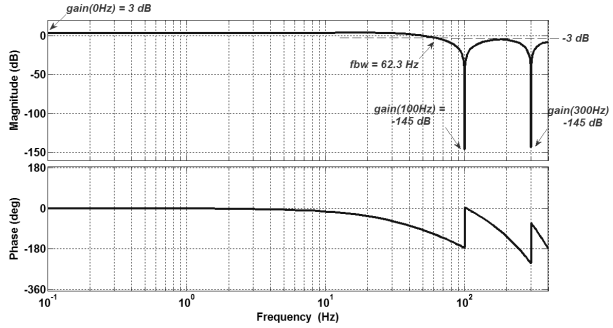

Fig. 8. Frequency characteristic of proposed PLL structure (without gain compensator).

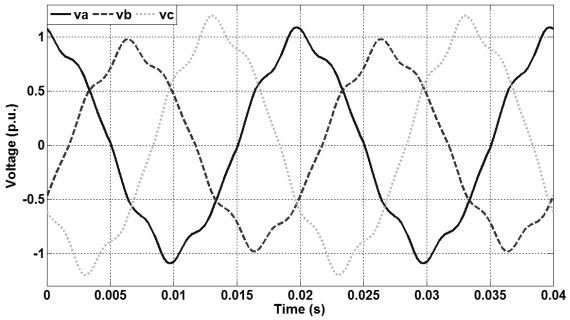

Fig. 9. Grid phase voltage waveforms used in simulation. Simulated unbalance is 10% and total harmonic distortion 7.07% (with 5th and 7th harmonics).

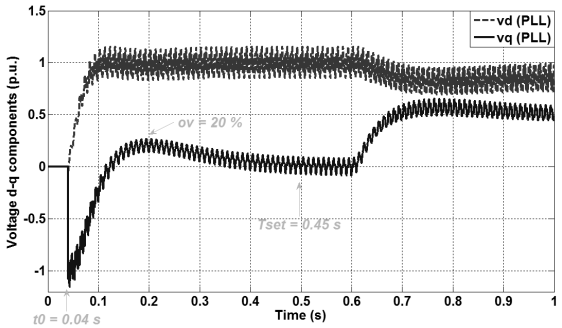

Fig. 10. d-q grid voltage components at the input of the conventional PLL system. Response to abrupt grid voltage phase shift of 60 degrees (at 0.6 s).

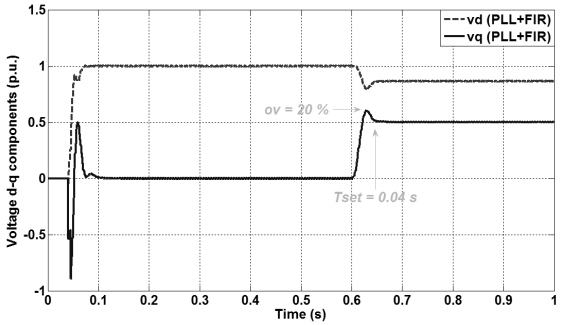

Fig. 11. d-q grid voltage components at the input of the proposed PLL with pre-filtering. Response to abrupt grid voltage phase shift of 60 degrees (at 0.6 s).

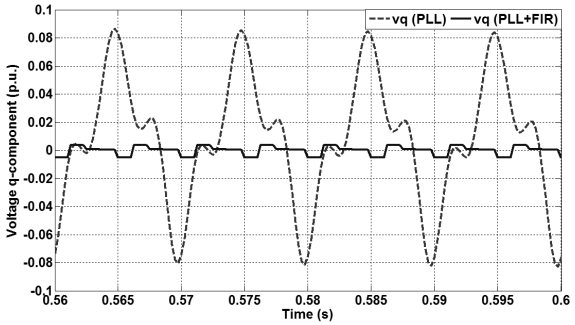

Fig. 12. Grid voltage q-component in conventional (dashed) and proposed (solid) PLL. 2nd and 6th harmonics are not propagated through proposed PLL.

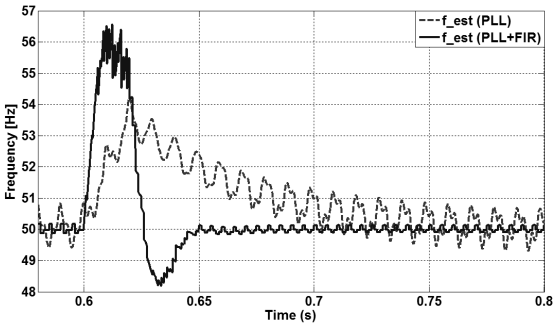

Fig. 13. Estimated grid voltage frequency in conventional (dashed) and proposed (solid) PLL. Proposed PLL gives faster response without harmonics.

steady-state when reference is set to 0. It verifies that the new system perform better compare to conventional where one can observe presence of 100 Hz and 300 Hz harmonic components. Such oscillations would propagate through the PLL filter which would result in the same oscillatory estimated frequency, as shown in Fig. 13. New system is more aggressive with higher overshoot in estimated frequency during transient (at 0.6 s in Fig. 13), but it settles much faster in about 2 fundamental periods and result in much cleaner frequency information without oscillations. Finally, Fig. 14 shows the estimation of the grid voltage phase angle using the proposed pre-filtered PLL. It proves that proposed PLL rejects the unbalance and harmonics effects, generating a clean synchronization signal (*theta_est)*, aligned to the amplitude of fundamental harmonic (*va_fund*) of distorted voltage in phase *a* (*va*).

Additionally, the proposed PLL system and its contribution to the control quality are tested considering entire voltage oriented vector control structure. In order to verify voltage oriented control principle and test its operation under unbalanced and distorted grid voltage conditions, detailed average model of space vector modulated (SVPWM) grid-connected voltage-source converter has been developed, according to Fig. 15. Parameters of the system are given in appendix.

Firstly, grid-side converter response to d-q current references was tested using conventional PLL (with set bandwidth 3 Hz). Figs 16 and 17 show obtained results with dashed lines. Till 0.04 s, d-q current references were set to

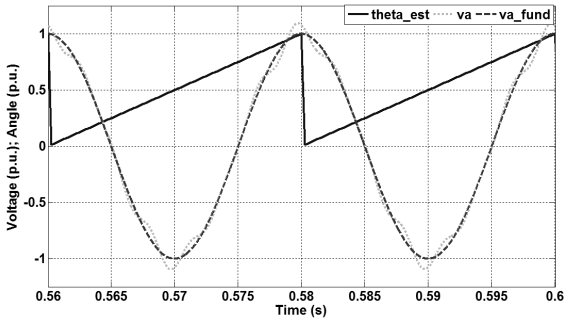

Fig. 14. Estimated grid voltage phase angle is clear and precisely aligned with fundamental harmonic of the grid voltage.

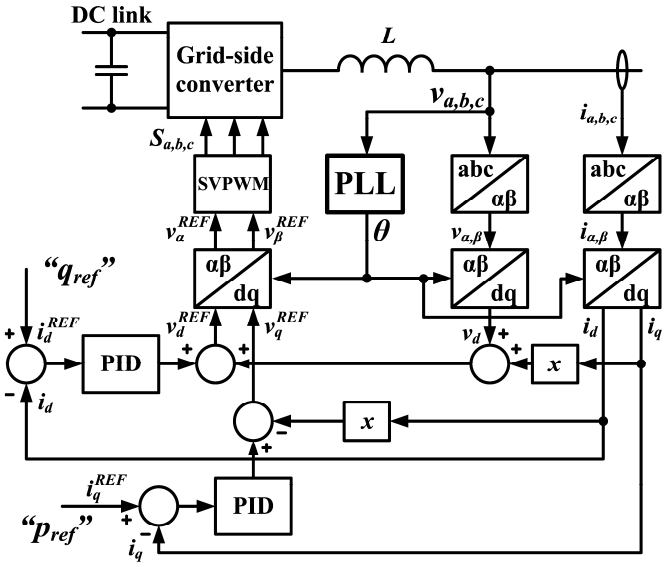

Fig. 15. Grid voltage oriented vector control structure for grid-side power converter. Independent control of active and reactive power is achieved.

zero, when q-current references determined active power to the grid is set to 0.5 p.u., and after that at 0.1 s d-current component determined reactive power is set to 0.3 p.u. Simulation showed that obtained current components contain characteristic harmonics at 100 Hz and 300 Hz with amplitude of 15 % (of fundamental signal). That results in distorted phase current waveforms, particularly in the region of its maximum values, which could be observed in Fig. 17. Here, it must be noted that besides PLL introduced errors additional influence on control quality also has d-q current controllers. Used current controllers are PI type controllers without any additional part charged for rejecting grid disturbances. Main goal was to observe how proposed PLL contribute to the quality control in terms of generated grid current distortion. Results using proposed PLL instead conventional are given in the same figures with solid lines. Obtained current oscillations are about twice reduced, using the same current controller gains. It results in more sinusoidal grid current waveform compare to the situation when conventional method was used (Fig. 17). Improvement comes exclusively from cleaner synchronization angle (without harmonic content) used for current transformation in d-q reference frame.

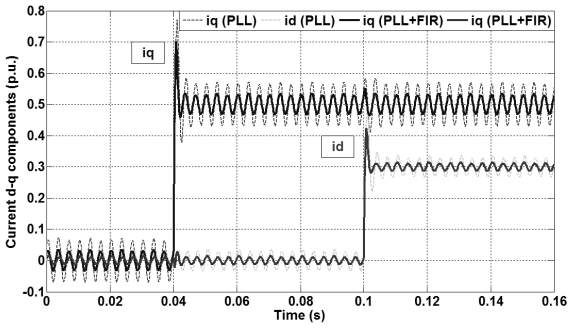

Fig. 16. Converter d-q grid current components and their response to current references when conventional (dashed) and proposed (solid) PLL is used.

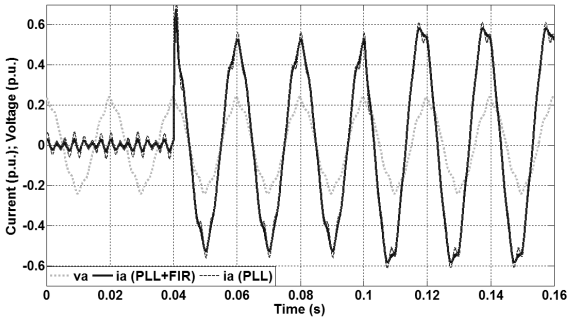

Fig. 17. Grid-side converter line current when conventional (dashed) and proposed (solid) PLL is used in control structure.

VII. Conclusion

This paper presented an improved pre-filter based PLL for phase angle and frequency estimation necessary for achieving proper vector control method in grid-connected converter applications. Proposed PLL method is especially suitable for application in highly unbalanced and distorted grid voltage conditions, because it is not subject to their influence. Therefore, authors consider it is appropriate for application in growing sector of distributed power generation systems based on renewable energy sources. Besides, proposed PLL method allows setting of much higher bandwidth then usual which is favorable in the case of grid voltage sags and frequency variations. Grid frequency variations and grid voltage offset are not considered in the paper. As fundamental grid frequency is not constant, certain coefficients in the FIR filter subsections must be recalculated on-line. Also due to the offset in voltage signals introduced by measuring devices, oscillation error at fundamental frequency would appear in the estimated phase angle and frequency. Their influence will be considered in some future work.

Appendix

Parameters of the system used in simulation: coupling inductance 7.5 mH, coupling resistance 0.26 Ω, grid voltage 212 V, DC-link voltage 580 V, current and PLL sampling frequency 4000 Hz, base voltage 960 V, base current 8 A, current controller gains K_P = 0.41 and K_{Iz} = 0.2, PLL filter gains K_P = 26.6 and K_{Iz} = 0.04 for f_{bw} = 3 Hz and K_P = 222.4 and K_{Iz} = 3.08 for f_{bw} = 25 Hz, PLL pre-filter sampling frequency 800 Hz.

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