Multi Channel ΣΔ A/D Converter for Integrated Power Meter

Dejan D. Mirković and Predrag M. Petković

***Abstract*—This paper describes three architectures for multi-channel sigma-delta ADC IC design. The proposed solution is aimed for the front-end of a three-phase integrated power meter. The pervious version of the power meter is to be redesigned by substituting six ADCs with two: one for converting currents and another for converting voltages in the three-phase power system. Therefore one pair of analog 3-to-1 multiplexers precedes ADCs. Discussion of advantages and drawbacks of the proposed solutions is illustrated by simulations using ADMS simulator that is a part of Mentor Graphics design kit.**

***Index Terms*—A/D converter, ΣΔ modulator, multiplexer, power-meter.**

I. Introduction

THE analog frontend of an integrated power meter is relatively small comparing to the digital part, especially when number of transistors is used as a measure. However, in all other aspects it represents the crucial part of the overall system on chip (SoC). The functionality of the system depends on the analog part. Moreover, even small inconsistencies in this block considerably ruin measurement characteristics of the SoC. Consequently designing of the analog part requires a lot of time, strict sticking to the design rules and a lot of designer's care and concentration.

In this paper we consider redesigning the front-end of three-phase solid-state power meter. Current version of the chip named IMPEG-2 has been designed in LEDA laboratory within Faculty of Electronic Engineering in Niš, Serbia. The new one is the third member of IMPEG solid-state power meter series. The first is IMPEG-1 dedicated for power metering in single phase power systems [1, 2, 3]. It consists of analog front-end, digital filters and DSP block as Fig. 1 presents.

The power meter is based on measurement of instantaneous values of voltage and current. They are sampled in two separated channels that consist of two SC oversampled ADCs

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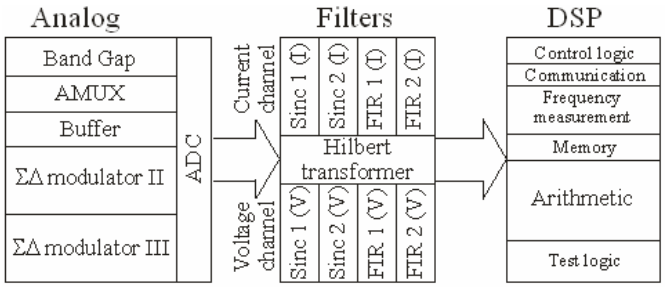

Fig. 1. Structure of IMPEG chip.

that launch digital filters and store data in corresponding registers. DSP block calculates active, reactive and apparent powers and energies. Accuracy of the calculated powers and energies mainly depends on precision of measured current and voltage.

IMPEG 1 was designed in 2003/04 and prototyped and tested in 2005.

Encouraged with the obtained results the LEDA team designed three-phase version of IMPEG in 2006/07. It differs from IMPEG-1 mainly in digital part. The analog front-end was triplicate of the analog part of the basic IMPEG version.

LEDA team is motivated to optimize area, power consumption and performances in the new variation of IMPEG. Therefore the digital part has been enriched with temperature self-calibration and low-power-driven design. The aim is to decrease area of the analog part replacing six ADCs with as few as possible. This paper analyses possible architectures for multichannel sigma delta A/D convertors.

The paper is organized as follows. The subsequent section describes architecture of IMPEG-2. The third section considers possible solutions for multiplexed AD converter and suggests type of architecture that fits the best to the specification. Thereafter, the behavior and performances of the chosen circuitry are verified in the fourth section.

II. IMPEG-2

IMPEG-2 represents three-phase version of IMPEG-1. However it is not plain triplication of the mono-phase version.

Fig. 2 represents the structure of IMPEG 2 [4]. The main differences are in digital part. Computation engine that has relayed on DSP block is accomplished with embedded MCU 8052. Besides, drivers for LCD display, real time clock, digital PLL, original acquisition block and converter for battery

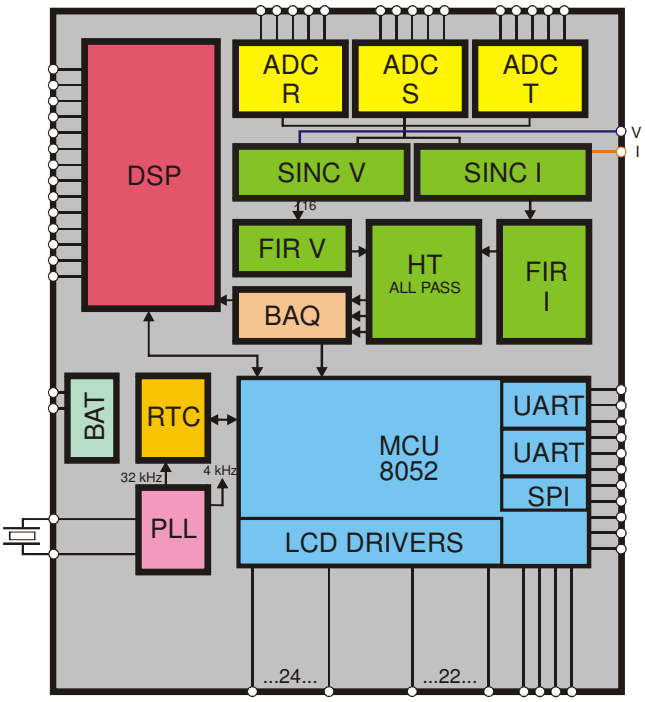

Fig. 2. Structure of IMPEG 2.

driven bias are incorporated as well. Moreover, major innovations have been made in digital filter block [5]. Namely, Sinc, FIR and Hilbert transformer filters implement compact MAC architecture and time multiplexing technique. As result the overall area for digital filters is increased only for 3% in comparison to the mono-phase realization. Practically, all three phases in voltage and current channel separately share the same hardware for digital filtering, as Fig. 3 shows.

Obviously, six sigma-delta modulators spoil the compactness of the solution. Therefore the next section considers possibilities for designing more compact solution. All of them are based on multiplexed approach.

III. MULTIPLEXED SD MODULATOR

The basic idea is to put as much channels as possible through the same ADC and avoid differences due to different offset, integral and differential nonlinearities and other ADC imperfectness. Besides, the goal is to spare chip area for as many modulators as possible without lost of functionality. Simultaneously it is desirable to retain already designed and tested full custom designed macro-cells. In the scope of analog frontend it means not to change the order of modulator and its basic blocks: integrators, opamps, band gap reference, quantizer and single-bit DAC.

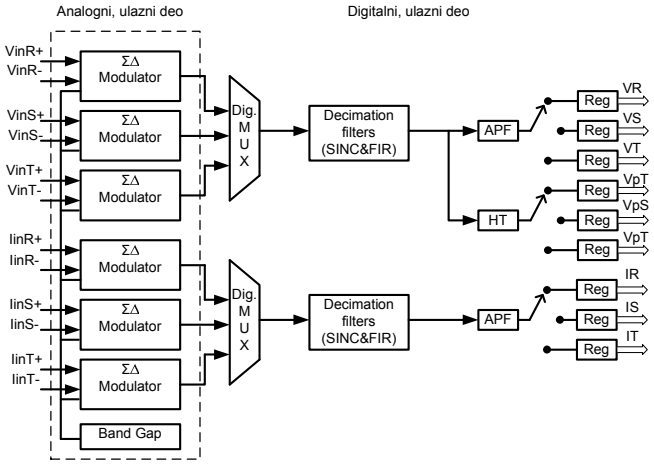

Fig. 3. ADC part of IMPEG 2.

The structure of used ΣΔ modulator is shown in Fig. 4 [3].

Integrators are realized using switch capacitor (SC) method [8]. Although differential architecture is practically used, for the sake of simplification it will be illustrated in single-ended version as Fig. 5. presents.

Observing Fig. 3 and Fig. 5 one can conclude that the most compact solution would be to replace all six modulators with one as Fig. 6 illustrates. The proposed architecture is inspired by [7, 8].

All six inputs, three for voltages of three phases denoted with VR, VS and VT and three for the corresponding currents denoted as IR, IS and IT comes to the input of multiplexer 6 to 1 (MUX6-1 in Fig. 6). However, to retain the same sampling frequency as the original circuit has (Fig. 3) and to persist in-phase sampling of all six signals, the multiplexer is driven from sample and hold circuits. All analog signals should be sampled with the same clock at frequency of 524288 Hz. The hold time should last long enough to allow conversions for all six channels. To accomplish this task one needs at least six times faster switching in modulator than the sampling frequency. Namely it requires clock of 3.14 MHz.

Digital signals are sent to the appropriate registers at the output where clock rate is returned to the sampling frequency rate of 524288 Hz. Therefore the rest of SoC will not be disturbed.

Knowing limitations of the used folded cascode operational amplifier of GBW=7.3 MHz and slew-rate of 5 V/μs [6], this means that the proposed architecture is close to the acceptable upper margins of the design.

Opposite solution is to multiplex only two channels: one for voltage and another for current within a single modulator. Three-phase power meter needs three such architectures, one for every phase. Supposing that sampling data rate remains 524288 Hz this implies that modulator has to be switched with rate of 1.05 MHz .This is below limits of implemented opamps and therefore a feasible solution. However the overall spare in area is less than 1/2 of the solution presented in Fig. 3.

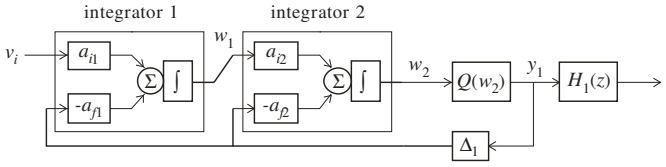

Fig. 4. Structure of second order ΣΔ modulator.

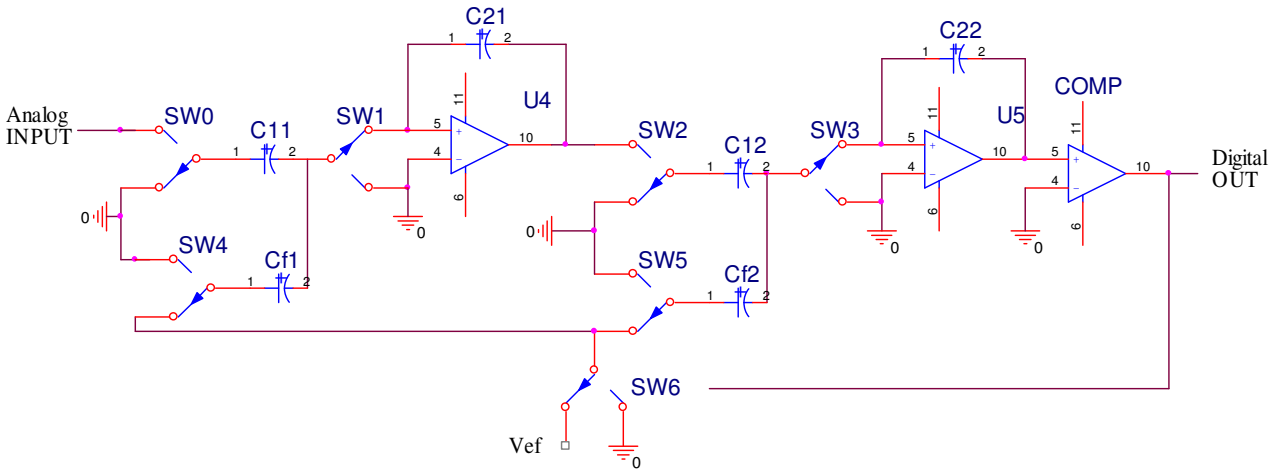

Fig. 5. Second-order ΣΔ modulator realized in SC architecture suitable for standard CMOS.

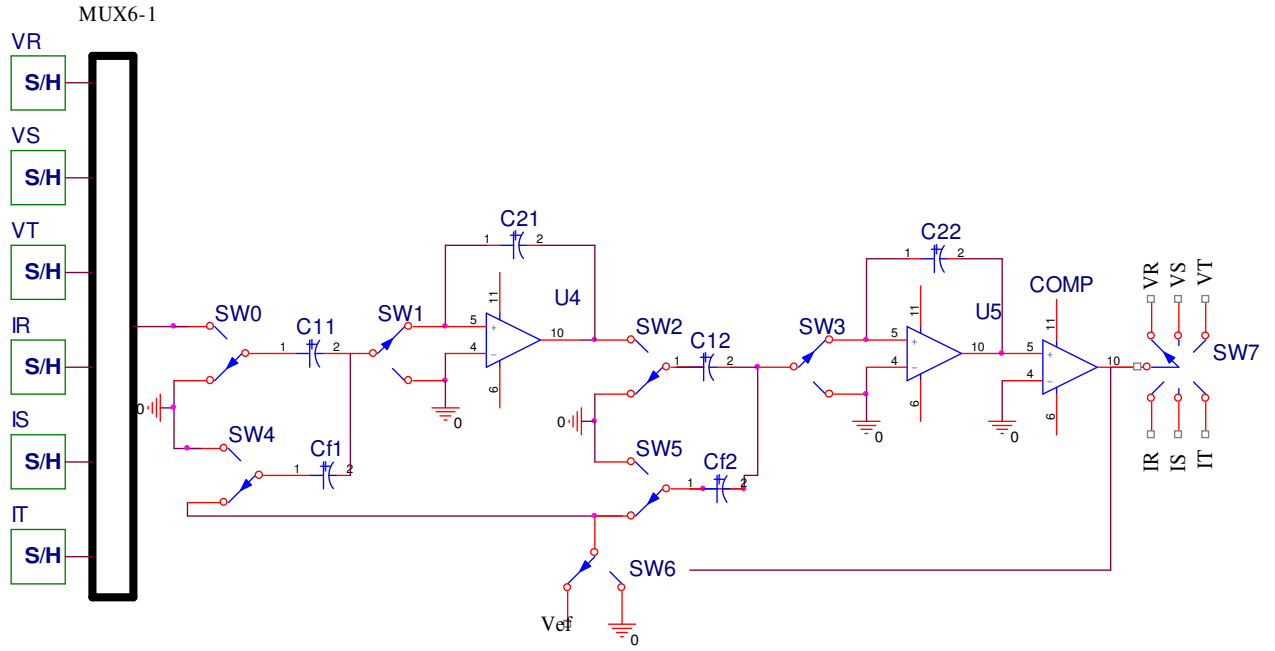

Fig. 6. Single second-order ΣΔ modulator with six multiplexed inputs/outputs.

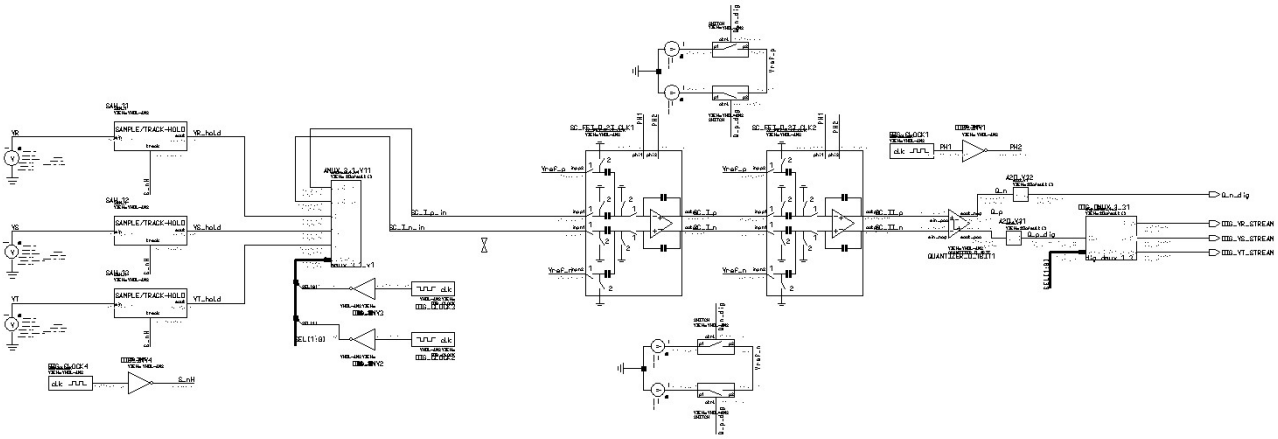

Fig. 7. Second-order differential ΣΔ modulator with three multiplexed inputs/outputs.

Although the number of ADC is decreased, the number of capacitors in C_{f1}, C_{f2}, C_{21} and C_{22} will be duplicated. However, due to the increased frequency the value of capacitances will be halved. Therefore the overall gain should be analyzed carefully. Besides, successive sampled values on SCs will differ considerably due to the different order of magnitudes and dynamic signal ranges in voltage and current channels.

The third solution for multiplexed ADC suitable for the integrated power meter consists of 3 to 1 multiplexer. The system requires two identical blocks, as Fig. 7 presents. One for three voltages (for each of three phases) whiles another being for three currents. Therefore it fits well to the general architecture presented in Fig. 3 because voltage and current channels are separated. This pursues the natural data flow to distinct digital filters and driven by different dynamic ratio in current and voltage channels. Moreover, for fixed sampling rate of 524288 Hz this requires moderately increased switching frequency of 1.57 MHz. The overall area will be shrunken less than 1/3 of the solution presented in Fig. 3. The decreased gain in area is caused by circuit complexity that is not shown in Fig. 5 to Fig. 7. Namely, although sizes of capacitors were shrunken, additional circuitry is needed to store previous sample for every channel.

IV. Simulation Results

The former architecture has been thoroughly verified by simulation.

Firstly, behavioral VHDL-AMS model has been developed and confirmed. It is used to check timing for S/H and two-phase clock signals needed to switch modulator.

Fig. 8 presents the accepted timing of clock waveforms. SH denotes switching in S/H circuits. Low logic level corresponds to the sampling phase while the high logic level defines the hold status. CLK1 and CLK2 denote controlling switching signals within modulator.

During high level of CLK1 input signal drives C11 and C12, while during CLK2 high the charge is transferred to C21 and C22.

Simulations confirmed expected functionality. Some of the representative waveforms are presented in the following figure.

Fig. 9 illustrates the obtained results for analog multiplexer. Sampled values of the corresponding input signals are presented at the output of analog multiplexer. The input of ΣΔ modulator is fed by this output.

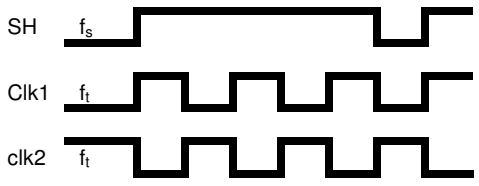

Fig. 8. Simplified timing diagram of driving signals in three input multiplexed ADC.

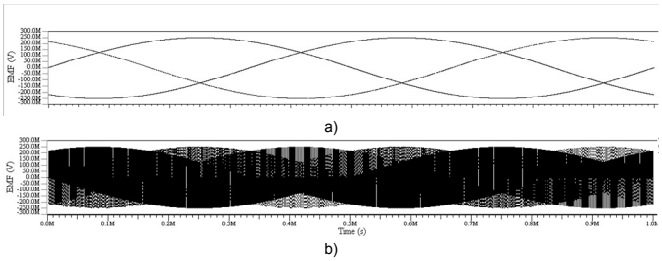

Fig. 9. Simulation results obtained for three channel architecture: input a), and output b) of analog multiplexer.

After modulation, signal is decimated using decimation filter with decimation factor of 128. Finally 19-bit word is obtained at the output of the converter. Fig. 10 represents the Fast Fourier Transformation of one of the converted outputs.

In this case effects of different kinds of noise (clock jitter, operational amplifier, KT/C) are taken into account. As result, suppression of harmonics is decreased, but still in the acceptable margins. For generating results presented in Fig 10. MATLAB is used as tool. Decimation filter and ΣΔ modulator with noise effects are modeled combining MATLAB scripting and Simulink test bench environment.

V. Conclusion

Three architectures for multiplexed ΣΔ ADC suitable for implementation within a three-phase solid-state power meter were discussed. All of them rely on using sampling-and-hold circuits at inputs to synchronize sampling of all input signals. The goal was to use as much of already designed analog and digital blocks as possible. Therefore it is necessary to sample SH circuits with the frequency of 524288 Hz and to obtain oversampled digital output with the same rate. This request can be fulfilled only if modulator switching frequency is increased as much as multiplexed signals are driven into it. This opens the issue of performances of used operational amplifiers and the issue of reliability of the overall SoC. Power

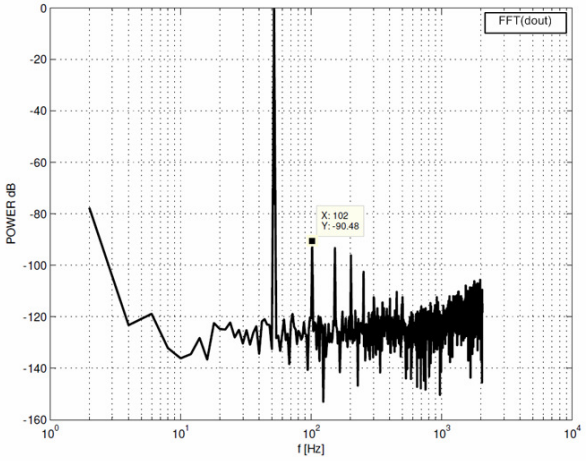

Fig. 10. FFT of one of the channels after decimation.

meter is expected to work persistently and reliably for at least ten years. Therefore it is better to design them to run in modest operation conditions. Timing properties of operational amplifier are crucial for achieving high frequency switching rate of modulator. Eventually it is better to trade small amount of chip area for more robust and reliable component.

As the modulator is realized in SC manner, the increase of switching frequency reflects to the component size. Namely resistors are realized as SC. Hence their value is defined with $T/2C$, where T is $1/f_{sw}$; f_{sw} being the switching frequency. Consequently the increase of f_{sw} requires smaller C for the same R. From other side, the bandwidth of the integrator is defined by RC product. Remaining the same RC can be achieved by decreasing C. In both cases dimensions of one of the implemented capacitors will be decreased. Moreover coefficients in Fig. 4 are defined as ratio of corresponding capacitances. Therefore if one is decreased, the other should be shrinking as well. Fortunately all this leads to the very slight modifications of layout. Namely, due to their dimensions, all capacitors are laid out as matched structures out of the modulator areas. This satisfies the basic request to reuse already designed macro cells.

However, the existing, previously tested opamp has precisely defined GBW and slew rate. This put boundary to the maximum switching rate.

Finally, the chosen solution is based on using 3 to 1 multiplexed ADCs. One is used for three voltages, another for the corresponding currents. This architecture match to the overall SoC concept that considers voltages and currents separately in order to protect sensible current channels from possible crosstalk produced in voltage channels. Moreover, this fits to the basic layout rule stressed in [9] “if it looks good, it will work”.

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