Efficiency Optimization Methods in Low-Power High-Frequency Digitally Controlled SMPS

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***Abstract*—This paper gives a review of several power efficiency optimization techniques that are utilizing advantages of emerging digital control in high frequency switch-mode power supplies (SMPS), processing power from a fraction of watt to several hundreds of watts. Loss mechanisms in semiconductor components are briefly reviewed and the related principles of on-line efficiency optimization through power stage segmentation and gate voltage variation presented. Practical implementations of such methods utilizing load prediction or data extraction from a digital control loop are shown. The benefits of the presented efficiency methods are verified through experimental results, showing efficiency improvements, ranging from 2% to 30%, depending on the load conditions.**

***Index Terms*—Low-power SMPS, efficiency optimization digital control.**

I. Introduction

In low-power SMPS supplying mobile devices, computers, as well as numerous other applications, digital controllers have emerged as an attractive alternative to traditionally used analog systems. The digital control offers flexibility and possibility for implementation of advanced control and power management techniques improving systems flexibility, dynamics, reliability, and power processing efficiency.

In here, the focus is on the techniques for improving the shape of the power processing efficiency curve by minimizing semiconductor losses. Conventional SMPS are usually designed to be the most efficient at the optimal operating point, defined for a specific load conditions. As a result their efficiency curve is not flat and at, certain loads, reduces to drastically low values. This presents a serious issue in modern low power systems, where the loads are frequently changing over a wide range. To minimize this problem, systems operating in two or three distinctive modes, and often combining switch mode and linear power supplies, have been developed [1]. In these systems, at medium and heavy loads the SMPS operating in continuous-conduction mode is usually utilized. At light loads, the SMPS operates in the discontinuous conduction mode, regulated through pulse-frequency modulation, and at very light loads the liner supply usually takes over. These 3-mode systems demonstrate a significant improvement of the efficiency curve over single-mode SMPS, but still have relatively large regions where the efficiency is poor.

This paper shows a set of digital-control based methods for further elevating the low efficiency regions and obtaining flatter efficiency curves. The following section briefly reviews sources of losses in low-power SMPS. In this paper, the emphasis is on the losses caused by semiconductor components that can be minimized through a design of power stage and controller, which in low-power SMPS are usually on-chip integrated and in the designer's control. In view of that, basic principles of efficiency optimization and implementation challenges are described. Sections III to V review several practical implementations of the efficiency optimization systems. In Section VI conclusions and a general comparison of the methods are given.

II. Sources of Semiconductor Losses and Principles of Optimization

Fig. 1 shows a general block diagram of a low-power dc-dc converter highlighting various sources of losses. In this SMPS, semiconductor losses are not only caused by the power switching components and gate drives but also by the power consumption of the controller itself. Due to low amounts of the processed power, in some cases, the consumption of the controller is comparable to the total amount of processed power significantly affecting the overall system efficiency. Also, in the case when a wide bandwidth current sensing circuit is used, such as in current programmed (CPM) mode

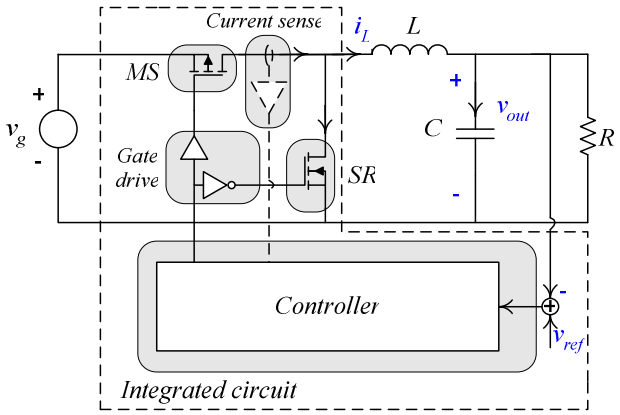

Fig. 1. A low-power dc-dc buck-based SMPS with highlighted sources of emiconductor losses (grey shaded areas).

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controllers the losses of the current sensing circuit can also be significant. Hence, a control circuit for improving efficiency needs to be implemented in a practical way, both in terms of the hardware complexity and the power consumption.

To review the task that a controller with efficiency optimization needs to complete, we can analyze the losses of power switching components.

Fig. 2 and equations (1) to (3) describe the sources of losses associated with the operation of the N MOSFET power transistor.

The losses of the gate drive circuit, P_{gate}, can be approximate as [2]:

$$P_{gate} = V_{gate} Q_g f_s \tag{1}$$

where V_{gate} is the gate supply voltage, Q_g is total gate charge seen by the driver, which is proportional to the transistor area, and $f_s = 1/T_s$ is the switching frequency of the converter.

The conduction losses of the transistor can be described as [2]:

$$P_{cond} = i_{rms}^2 R_{ds} \tag{2}$$

where

$$R_{ds} \approx \frac{R_{ds\_o}}{K(V_g - V_{th})}, \tag{3}$$

in (3), V_{th} is the threshold voltage of the transistor, and K is a construction constant that, for a given length, determined by the brake down voltage, is inversely proportional to the transistor area.

It can be seen that both conduction and switching losses, depend on the transistor's sizing and the gate supply voltage. Ideally, in order to maximize the efficiency, the optimizing controller needs to change one or both of these two parameters, such that, for any given operating condition, the sum of P_{cond} and P_{gate} is minimal. Accordingly, the efficiency optimization methods that, generally, can be categorized in dynamic power stage segmentation and gate voltage variation based have been developed.

In segmentation based methods, the complete power stage or just semiconductor switches are divided into parallel segments and, depending on the load conditions, the number of active segments is changed in time. Gate voltage variation based methods dynamically change V_g to achieve the same effect.

From the previous discussion the task of the optimizing controller can be recognized. It usually needs to "recognize" operating condition in the circuit and, accordingly, reconfigures the power stage and/or adjust gate drive voltage, such that the losses are minimized.

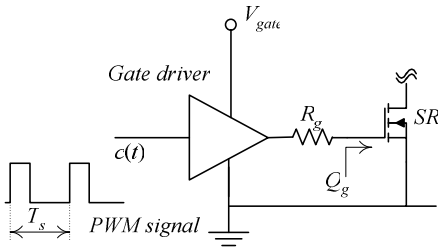

Fig. 2. N-MOS transistor and gate drive circuit.

III. Single Phase Current Programmed Mode Controller with Optimization

In the current programmed mode controller (CPM) [3] of Fig. 3, information about the load conditions in the circuit is extracted from a control loop and consequently utilized for efficiency optimization.

In this implementation [4], both the segmentation and gate-voltage variations are utilized. It can be seen that the power switches and gate drive circuit are separated into several parallel segments that can be controlled independently. The controller consists of two feedback loops, outer voltage loop implemented in a digital fashion, and the inner current loop that is analog.

The output voltage regulation is performed like in a conventional current programmed mode (CPM) regulator. Based on the difference between the output voltage and the reference, i.e. voltage error $e[n]$, the voltage loop compensator creates a digital signal proportional to the peak inductor current $i_c[n]$. This digital value is then converted to an analog equivalent by a 1-bit Σ-Δ digital-to-analog converter, whose structure is fairly simple.

The efficiency optimization is performed as follows. Based on the value of $i_c[n]$, the segment selector of Fig. 1 changes the mode of SMPS operation between 4 distinctive modes, such that the losses are minimized. The first mode of operation is designed for heavy loads, where the conduction losses are dominant. In this mode all of the power switches are active increasing the total transistor area and minimizing R_{ds} (3) of the power switches. In the second mode, for medium loads, where the switching and conduction losses are comparable, only one or two segments are active. In both of the previous two modes the gate supply voltage is at its maximum minimizing the conduction resistance. The third mode of operation is at light loads, in the region where the switching losses are becoming larger than those due to the conduction. Here, only one segment is active and the gate supply voltage dynamically changes to reduce the contribution of the switching losses at the expense of minor increase in the conduction losses. This change is performed through the gate swing controller and switch capacitor circuit (Fig. 3) providing a set of constant voltage levels. The fourth mode of operation is reserved for even lighter loads. In this mode the gate supply voltage is at the minimum level and the output voltage regulation is done through pulse frequency modulation (PFM). To initiate PFM operation the peak current controlling reference $i_{cnt}[n]$ is set at a value lower than the equivalent of the inductor current ripple. Also, instead of clocking RS latch with an external clock at the switching frequency, in the fourth mode, the latch is clocked by the ADC. As soon as the error signal becomes larger than 1 it produces a clocking signal for

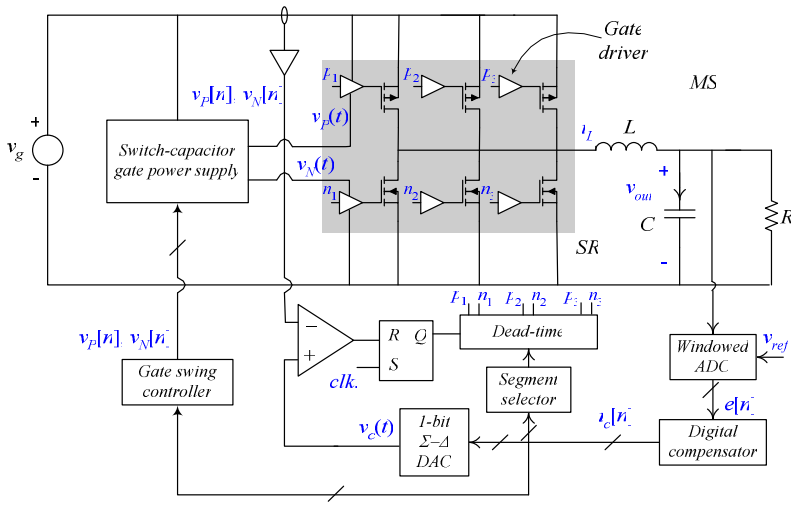

Fig. 3. Mixed-signal current programmed mode controller with efficiency optimization.

the latch.

Fig. 4 shows a comparison of the power processing efficiency between the previously presented system and a conventional CPM controlled SMPS without optimization. It can be seen that the efficiency improvement of this method depends on the operating point and ranges between few percent and more than 30%, at light loads.

It should be noted that, unlike the voltage controlled based methods discussed in the following sections, this method always guarantees that during load transients the SMPS always operates with the proper number of segments for a given instantaneous current. However, this comes at the price of a high gain bandwidth current sensor, which for some very low power high-frequency SMPS is too costly, both in terms of silicon area utilization and power consumption.

IV. Voltage Mode Controllers with Efficiency Optimization

In a typical voltage mode controlled low-power SMPS a current sensing circuit providing information about instantaneous current is usually unavailable. Hence, to obtain information about the current, in the two system presented here estimation is used. In both cases, the structure of the power stage, gate drivers, and the gate swing circuits can be similar to the one shown in Fig. 3.

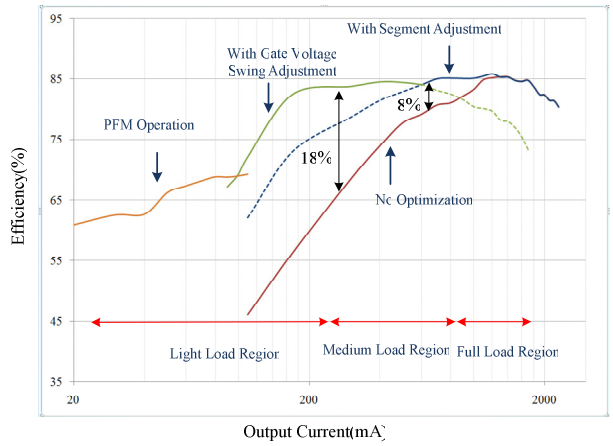

Fig. 4. Power processing efficiency comparison of a 2 A dc-dc buck converter.

A. Duty Ratio Based Optimization

The system of Fig. 5 uses information about duty ratio variation from its ideal value to estimate the load [5], and consequently, adjust the mode operation optimizing efficiency. The controller uses the fact that in a realistic SMPS the duty ratio $d[n]$ varies from its ideal due to the losses in the circuit and is usually proportional to the output load. The calculation of this discrepancy is performed with a slow ADC and an ideal duty ratio calculator, which based on the input and output voltage computes the ideal duty ratio value D_{ideal}, i.e. V_{ref}/V_g for a buck converter.

Since in most dc-dc converter input voltage usually changes slowly it is possible to use a slow and simple ADC. This method is suitable for a crude estimation of the mode of work and steady state operation.

Main limitations of such an efficiency optimization system are low precision of current estimation and a limited bandwidth. The estimation depends on the parasitic resistances and other loss contribution elements that change in time and

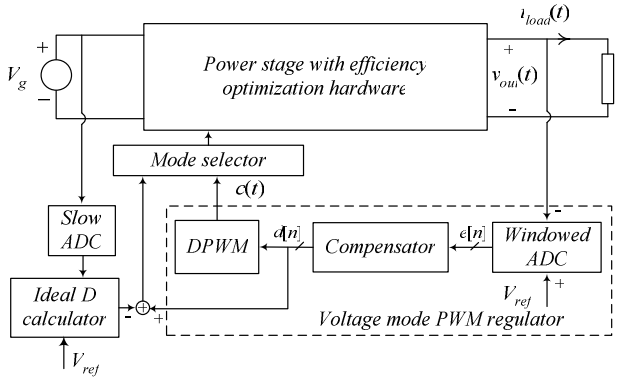

Fig. 5. Duty ratio based optimization system.

depend on the operating conditions. Also, it is highly inaccurate during load transients when, due to the compensator action, the duty ratio changes drastically.

B. Load Communication Based Predictive Efficiency Optimization

Compared to the previously presented method, a significant improvement of the speed and accuracy of the current estimation can be achieved if, to the certain extent, behavior of the load is known. The load predictive optimizer of Fig. 6 is designed for applications where the load depends on a digital data stream $s[n]$ that is fed to it. Examples include modern audio amplifiers [6], video equipment, small motors of portable devices, and other systems processing digital data streams in a predictable fashion. Here, a load predictor emulating transfer function $i_{load}[n]/s[n]$ is added to the conventional voltage loop allowing mode selector to react timely to frequent load changes.

It should be noted that, even thought, this system provides much more accurate current estimation its accuracy is still limited with the accuracy of the model used in the estimator construction.

Drawbacks of the both voltage mode methods presented here are related to a limited speed of the estimation and inaccuracy. Hence, a special attention needs to be devoted to the protection of power stage from current overstress. To eliminate situations where a small number of segments conduct a large current, possibly occurring during load transients, in these methods during each light-to-heavy load change all transistors of the segmented power stage are usually turned on. As a consequence, for highly dynamic loads the voltage mode system might be operating in suboptimal conditions over large time periods.

V. CPM Based Multi-Phase Converter with Logarithmic Current Sharing

In multiphase dc-dc systems the segmentation of the power stage is done such that several converters are operating in parallel. Due to cost constrains, implementation of the system with separate current sensing circuit in each phase is considered impractical

The principle of operation of the system with logarithmic current sharing [7] is described with Fig. 7.

The system consists of N parallel stages and operates on a similar principle as the $R/2R$ digital to analog converter

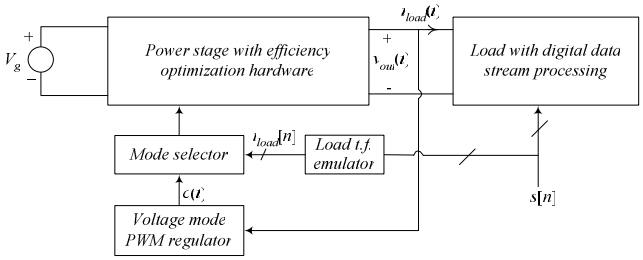

Fig. 6. Load prediction based efficiency optimization system.

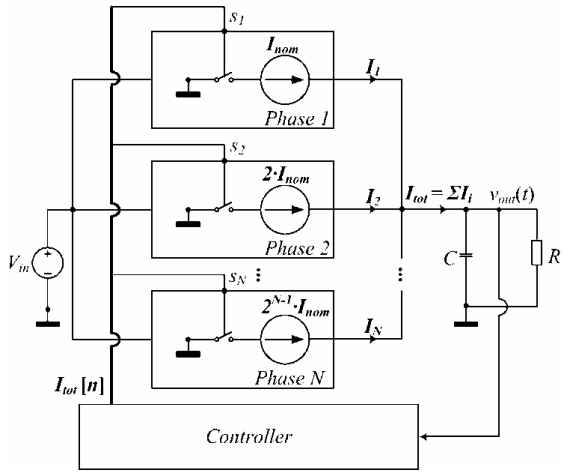

Fig. 7. Multi-phase CPM converter with logarithmic current sharing.

eliminating the need for a large number of current sensing circuits. Its parallel stages have currents that are rated in a binary logarithmic fashion. Each of the converters operates at a fixed peak efficiency point. To maintain the high efficiency over the full range of operation the binary weighted power stages are turned on and off, depending on the load requirement.

Practical implementation of this system is shown in Fig. 8. It can be seen that the controller operates in a similar fashion as the current program mode controller described in Section III. The digital voltage loop again creates a current reference, which is proportional to the load current. This current is formed by directly enabling and disabling binary weighted phases without a need for implementing a current sensor in each of the phases. The states of the phases (active or inactive) are controlled directly, by $i_{cnt}[n]$ signal in the following fashion: Its most significant bit (MSB) is connected to the largest phase, MSB-1 is connected to the second to largest phase, MSB-2 bit controls the second to largest phase, and so on.

In addition to the phases that are only operating in on or off state, with constant current, one phase equal to the smallest on/off phase and operating in an ordinary fashion, with current sensing circuit is added.

This phase provides tight output voltage regulation without the need for a large number of parallel phases. Compared to conventional multi-phase converters, the logarithmic system has a higher and flatter efficiency curve virtually over the full range of operation.

VI. Conclusions

In this paper optimization principles based on power stage segmentation and gate drive voltage variation for low power dc-dc are presented. Several practical implementations of the controllers with efficiency optimization are shown. A brief comparison between voltage and current program mode controlled techniques is given. Benefits and limitation of the methods are also presented.

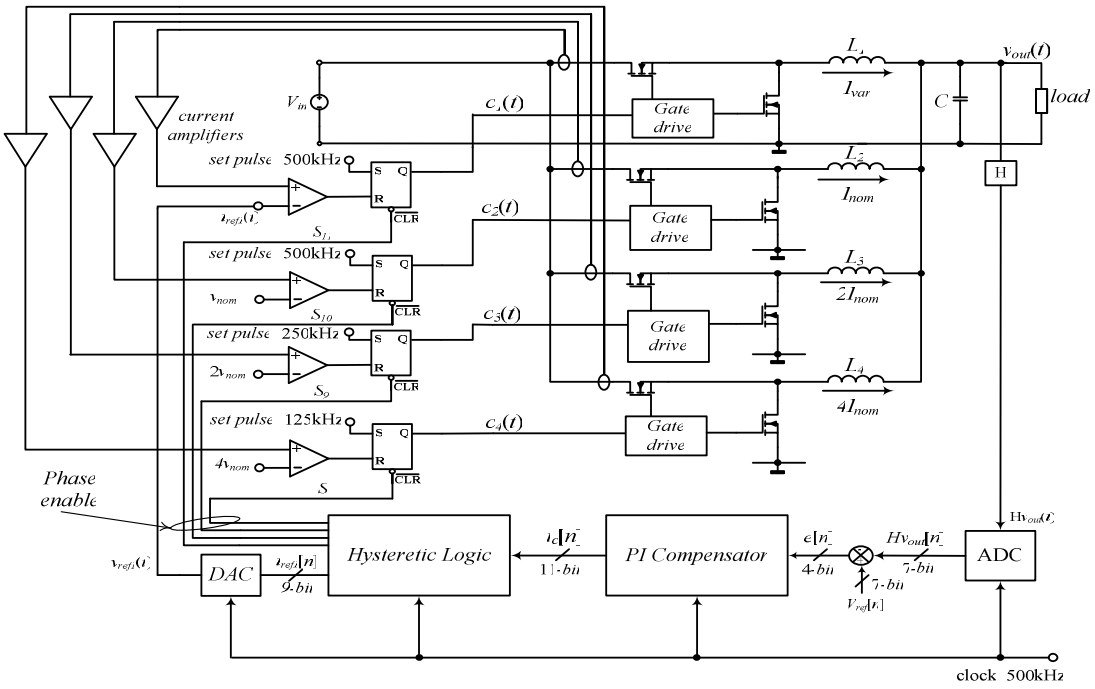

Fig. 8. Practical implementation of the multi-phase system with logarithmic current sharing.

REFERENCES

[1] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "An ultra-low-power digitally-controlled buck converter IC for cellular phone applications," Applied Power Electronics Conference and Exposition, APEC '04. IEEE, Vol. 1, pp. 383–391, 2004.

[2] S. Musuniri and P. Chapman, "Improvement of light load efficiency using width-switching scheme for CMOS transistors," Power Electronics Letters, Vol. 3, No. 3, pp. 105–110, 2005.

[3] R.W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," 2nd ed. Boston, MA: Kluwer 2000.

[4] A. Parayandeh,C. Pang, A. Prodić, "Digitally Controlled Low-Power DC-DC Converter with Instantaneous On-Line Efficiency Optimization," in Proc. IEEE APEC Conf, March 2009.

[5] A. Prodić and D. Maksimović, "Digital PWM Controller and Current Estimator for a Low-Power Switching Converter," in Proc., IEEE Computers in Power Electronics Conference (IEEE COMPEL), July 2000, pp. 123−128.

[6] O. Trescases, G. Wei, A. Prodić, W.T. Ng, K. Takasuka, T. Sugimoto, and H. Nishio "A Digital Predictive On-Line Energy Optimization Scheme for DC-DC Converters," in Proc. IEEE APEC Conf, March 2007.

[7] Z. Lukić, Z. Zhao, and A.Prodić, "Digital Controller for Multi-Phase DC-DC Converters with Logarithmic Current Sharing," in Proc. IEEE PESC, June 2007, pp.119−123.