A Half Bridge Inverter with Ultra-Fast IGBT Module – Modeling and Experimentation

Dinko Vukadinović, Ljubomir Kulišić, and Mateo Bašić

Abstract—**This paper presents an operation analysis of a single-phase half bridge inverter with ultra-fast IGBTs (insulated gate bipolar transistors) and freewheeling diodes (module SKM100GB125DN, manufactured by Semikron). The Simplorer software package, which is especially suitable for electrothermal modelling of power electronics circuits, was used for inverter operation modelling. In addition, a laboratory setup of the inverter was built in order to experimentally verify simulation results. The control unit of the inverter consists of a stabilised power supply, SG3525A pulse-width modulator and SKHI22B hybrid dual driver. At the same time, the abilities to change the transistor switching frequency and dead time are provided. Good agreement of the simulation and experimental results was confirmed.**

Index Terms—**Power electronics, IGBT, Inverter, Modeling.**

I. Introduction

It is well known that modern closed-loop electromotor drives for induction machine control are designed with three-phase inverters with IGBTs driven by pulse width modulation (PWM) principles. In these drives, IGBTs work as switches. However, transistors are not ideal switches, and they have certain turn-on and turn-off times. In this case, a dead or lock-out time should be provided between the switching of the devices in a leg of the inverter to prevent a shoot-through. Usually, the dead time is within 2-5 μs ([1]). As the dead time increases, the current ripple of the stator current of an induction motor becomes higher. One modern research topic in the field of industrial automation is development of compensation techniques to eliminate effects caused by this dead time. Advanced dead time compensation techniques include knowledge of the forward conduction voltage drop of the transistor and freewheeling diode. The difference between the target and actual phase voltage of an induction motor supplied by the voltage-source inverter can be given as ([2])

$$\Delta u = \frac{t_d + t_{on} - t_{off}}{T_c}(u_B - u_T + u_d) + \frac{u_T + u_D}{2} \qquad (1.1)$$

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where
t_d – the dead time of an inverter,
t_{on} (t_{off}) – the turn on (turn off) time of the transistor,
T_C –the PWM carrier period,
u_B – the DC-link voltage,
u_T – the forward conduction drop of the transistor and
u_D – the forward conduction drop of the diode.

Dead time effect compensation techniques are complex because the conduction drops in the transistor and in the diode depend on the related current and temperature of the semiconductor. IGBTs are usually chosen by the forward conduction current, which is two times higher than the nominal motor current, for short-time overloads ([3]). In this case, the conduction drop across the transistor depends significantly on the conduction current (visible from the data sheet for module SKM100GB125DN [4]), which results in more complex dead time effect compensation techniques and in a more expensive DSP (digital signal processor) to carry out this compensation.

As a first stage in the research of the dead time effect, a laboratory setup of a half bridge inverter with IGBTs was built. The half bridge inverter is only used in power circuits for DC/AC power conversion. One leg of the three-phase inverter is identical to one leg of the half bridge inverter, and hence problems existing in the half bridge inverter are common in three-phase inverters. For this reason, the half bridge inverter will be investigated, and the results can then be applied to three-phase PWM inverter analysis.

The laboratory setup was designed with IGBTs rated at 100 A, while load currents between 0.5-2 A were observed. Hence, the power transistor is deliberately oversized. Over this current range, the turn-off and turn-on times and the temperature influence are negligible. Given that the price of the transistor module made by Semikron in the Croatian market is less than 70 EUR, the proposed technical solution is economically justified.

II. Half Bridge Inverter with R-L Load

Fig. 1 shows the half bridge inverter with a resistive-inductive (R-L) load.

The related current and voltage waveforms are shown in Fig. 2. In this section, the ideal inverter is explained, where non-idealities of the components and parasitic effects are neglected.

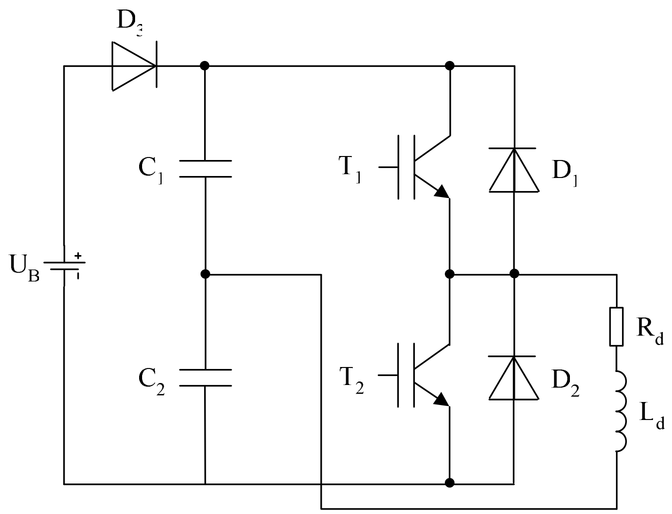


Fig. 1. Half bridge inverter with R-L load.

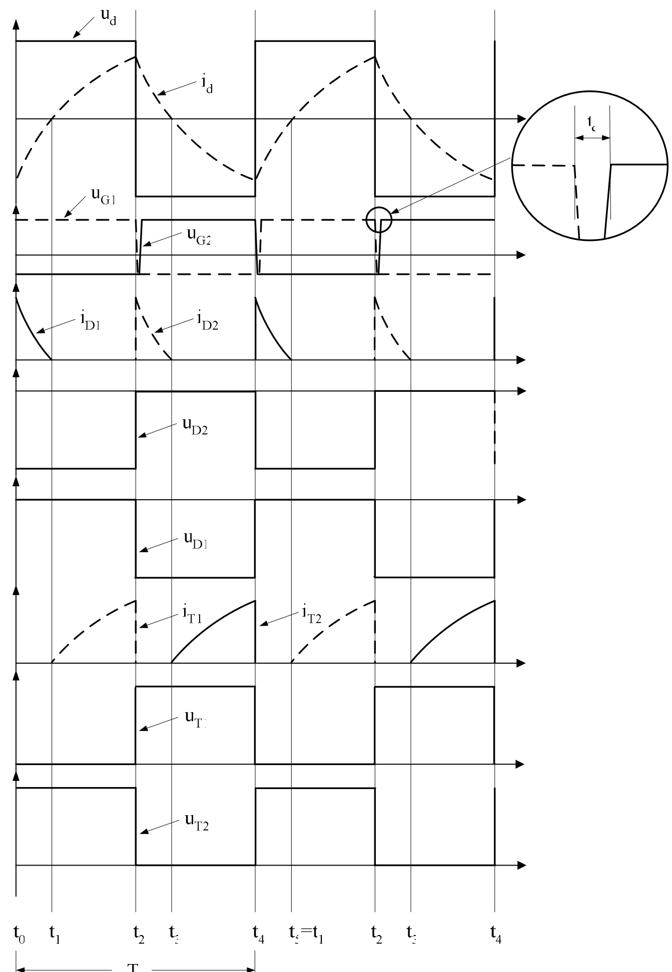


Fig. 2. Current and voltage waveforms of half bridge inverter.

The analysis of this inverter is given according to certain time intervals as the following.

The time interval (t_1, t_2): The transistor T_1 is turned on by a current pulse applied at the gate during the time interval $t < t_1$. However, the transistor T_1 will not conduct until t_1, when the load current i_d becomes zero, i.e. when the magnetic energy accumulated in the inductance L_d is discharged. Because the load circuit includes an inductance, the load current cannot instantly reach its steady state value. The current increase is defined by the load, i.e. R_d and L_d. During this time interval, the reverse voltage across the diode D_2 is U_B. The voltage across the transistor T_2 is U_B, and it blocks voltage.

The time interval (t_2, t_3): At time t_2, a driver turns off the transistor T_1, and the blocking voltage U_B lies across it until time t_4. It is clear that the pulse U_{G1} reaches negative value in order to ensure fast turn off of the transistor. At time t_2 the load current switches from the circuit C_1-T_1-R_d-L_d to the circuit C_2-D_2-R_d-L_d. During turn-off, because of the magnetic energy accumulated in the inductance L_d, the load current retains the same direction. The diode D_2 starts to conduct, because the conducting conditions are fulfilled until time t_3. The diode D_2 is reverse biased. At the end of the turn-off of the transistor T_1 it is necessary to ensure the dead time t_{dead}. The dead time t_{dead} prevents shoot-through, i.e. the incoming transistor should be delayed by a dead time from the outgoing transistor. At the end of the dead time t_{dead}, the transistor T_2 is triggered to turn on. Although the transistor fulfils conditions to forward conduct, it will not conduct until the load current falls to zero, at time t_3. As the load current i_d reaches zero value, the current changes its direction, and the next time interval starts.

The time interval (t_3, t_4): At time t_3 the load current changes its direction. As the transistor T_2 is able to conduct, the current starts to flow through the circuit C_2-L_d-R_d-T_2. The transistor T_2 conducts until time t_4 when it will be triggered to turn off.

The time interval (t_4, t_5): Immediately after turn-off of the transistor T_2 it is necessary to ensure the dead time before the incoming transistor is turned on. Then, the transistor T_2 blocks voltage. The load current flows through the diode D_1 until time t_5 when the current reaches zero value. When the current reaches zero value, it flows through the transistor T_1, and the overall process is repeated.

III. Simplorer Simulation of Half Bridge Inverter

Simplorer is a multipurpose program for designing electrothermal high performance systems ([5]). It was developed, primarily, for automation, the airline industry, automotive design and power electronics. Simplorer is among the first simulation tools to implement electrothermal models of power semiconductors at device level. It offers three levels of the simulation model complexity.

In this paper, we have chosen the advanced dynamic of the inverter model including freewheeling diode. The simulation parameters are the following ([6]):

- The electric parameters of the circuit: supply voltage U_B = 48 V, gate resistors $R_{G1} = R_{G2}$ = 12 Ω, capacitors $C_1 = C_2$= 1000 µF.
- The trigger voltage: trapezoidal voltage waveform, with amplitudes +15 V and -7 V, frequency f = 1.2 kHz; rise time is t_r = 1 µs, fall time t_f = 1 µs, dead time t_{dead} = 3.9 µs.
- The load: R_d variable between 0-50 Ω, L_d variable between

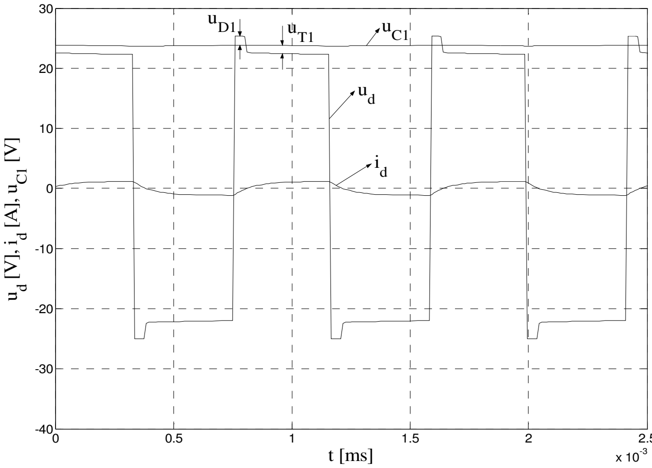


Fig. 3. Waveforms of load voltage, load current and voltage across the capacitor C_1; R_d =19 Ω, L_d = 1.5 mH.

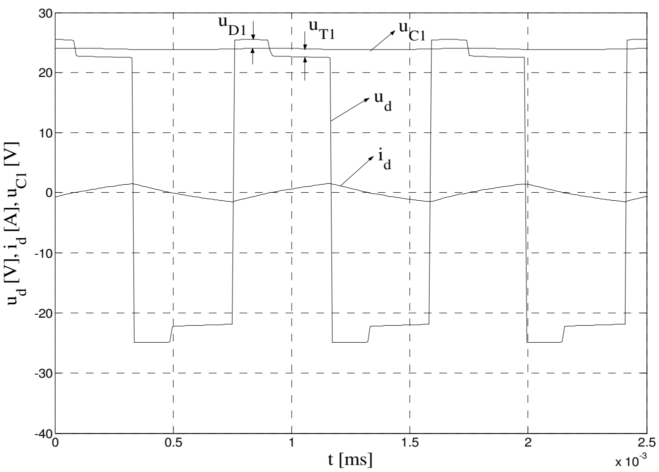


Fig. 4. Waveforms of load voltage, load current and voltage across the capacitor C_1; R_d =19 Ω, L_d = 1.5 mH.

1-52 mH.

Figs. 3 and 4 show the waveforms of the current and voltage of the variable resistive-inductive load and the voltage across the capacitor C_1 as well.

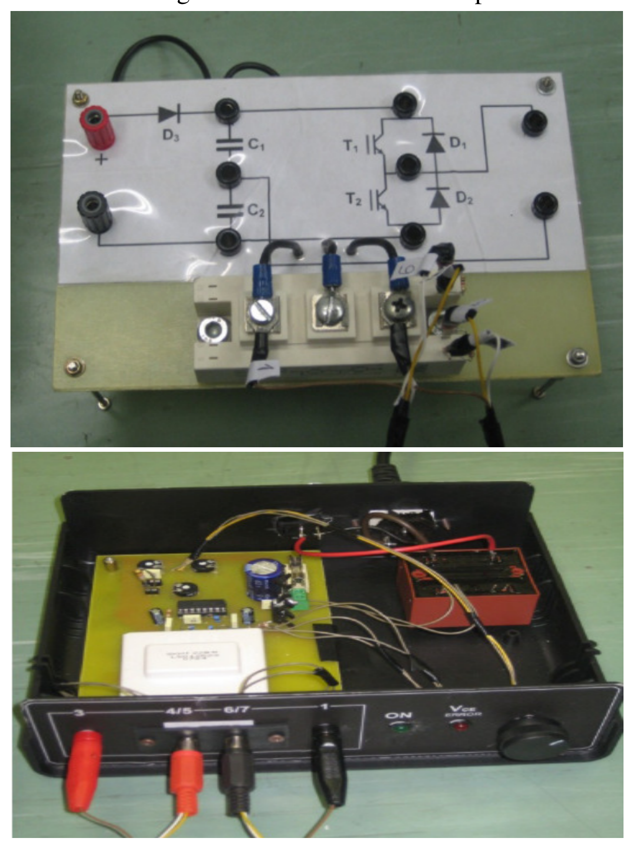
By comparison of the waveforms shown in Figs. 3 and 4 with the ideal waveforms shown in Fig. 2, it can be concluded that the load voltage does not have an ideal rectangular form. The amplitude of the load voltage u_d is not constant during the whole half-cycle. This amplitude is visibly higher when a diode conducts than when a transistor conducts. The reasons for this are the forward conduction voltage drops across diodes and transistors. The voltage drop across real IGBTs is usually between 1-3 V, and across diodes it is usually 1 V ([1]). When the transistor T_1 conducts, the load voltage is equal to the voltage across the capacitor C_1 ($\approx U_B/2$) minus the voltage drop across the transistor T_1 (Figs. 3 and 4). In the observed cases, the forward conduction voltage drop of the transistor u_T is 1.4 V and can be considered as constant over the observed current range. In a similar manner, the forward conduction drop of the diode D_1 is equal to the voltage across the capacitor C_1 plus the voltage drop across the diode D_1 (approximately 1.4 V in the observed cases).

IV. Laboratory Setup

In order to experimentally verify the theoretical investigations, the laboratory setup of the half bridge inverter was built in the Laboratory of Power Electronics of the Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture in Split. Specifications of the setup and the experimental results are presented in this section.

A. *Electric Scheme and Specifications of the Inverter*

The half bridge inverter consists of the power section and the control unit. The power section includes: the IGBT module with freewheeling diodes (D_1 and D_2), made by Semikron, type SKM100GB125DN, the capacitor of 1000 μF and the diode type BY255 (D_3). The photo of the power section and the control unit is shown in Fig. 5.



a)

b)

Fig. 5. Power section a) and control unit b) of inverter.

The control unit controls the half bridge inverter by triggering pulses. The rectangular waveform of these pulses is determined by the amplitudes of +15 V and -7 V. The set requirements to the control unit are to ensure two outputs, as they are 180 degrees out of phase with variable frequency, for each transistor separately. In addition, the adjustment of the dead time between the two signals must be ensured. In this paper, the set requirements for the control unit are carried out by the integrated circuit type SG3525A, which presents a pulse width modulator, and the integrated circuit SKHI22B, which presents a dual IGBT driver. In order to ensure the proper

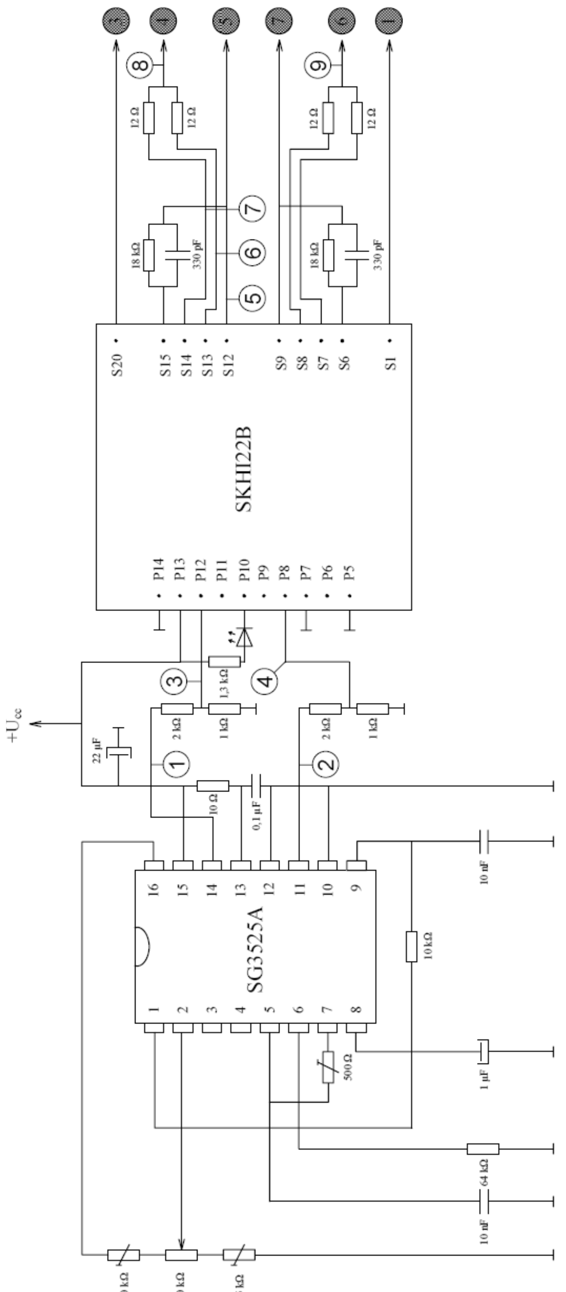


Fig. 6. Electric scheme of control unit.

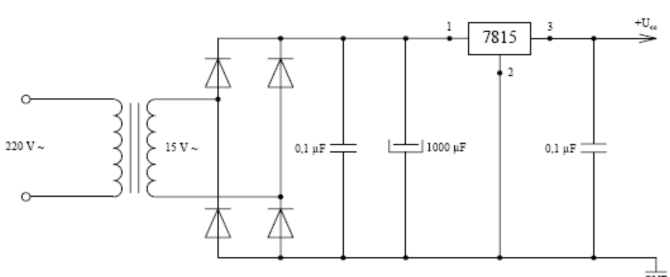


Fig. 7. Electric scheme of controlled voltage source.

operation of the control unit it must be supplied by the controlled voltage source. The electric scheme of the control unit is shown in Fig. 6, and the electric scheme of the controlled voltage source for the control unit supply is shown in Fig. 7.

The controlled voltage source shown in Fig. 7 includes: the power transformer, the diode bridge rectifier, the capacitor as an output filter and the series voltage regulator type 7815. Using this regulator on the output side of the rectifier, the stabilised voltage source of U_{CC} = +15 V is ensured.

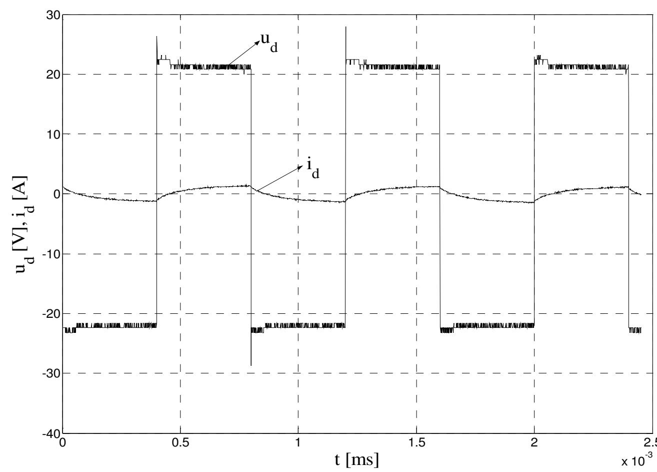


Fig. 8. Load voltage and current waveform; R_d =19 Ω, L_d = 1.5 mH.

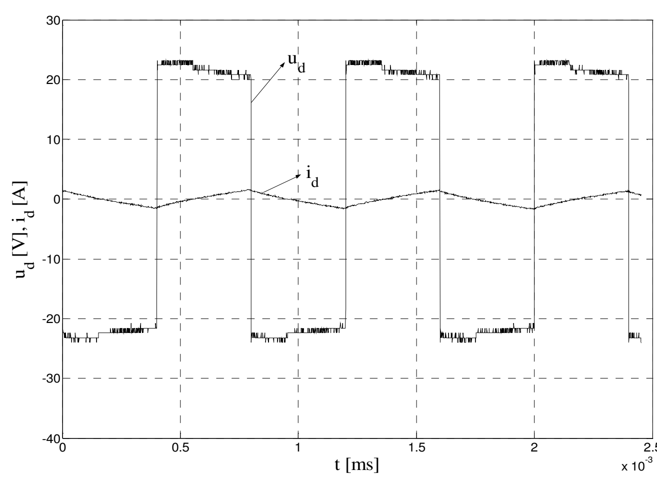


Fig. 9. Load voltage and current waveform; R_d =5 Ω, L_d = 3 mH.

B. Experimental Results

Figs. 8 and 9 show the experimental waveforms of the current and voltage of the resistive-inductive load obtained in the same operation modes and for the same parameters of the load as in Figs. 3 and 4.

The simulation results shown in Figs. 3 and 4 are in good agreement with the experimental results shown in Figs. 8 and 9, verifying the Simplorer model. The load voltage amplitude shown in Figs. 8 and 9 is approximately 2.5 V lower than the load voltage amplitude shown in Figs. 3 and 4 (during the forward conduction of both transistor and diode). The explanation for this effect is the following: the real battery used has an inner resistance, so the output voltage of the battery is the no-load voltage of the battery (48 V) minus the voltage drop across its inner resistance. This voltage drop is higher as the load current increases. Because of this, when a transistor forward conducts, the load voltage varies by a 0.4 V. Therefore, this voltage variability is caused by the non-ideal voltage source and not by the output characteristic of the transistor as in conformity with its data sheet ([4]). The variability of the load voltage during forward conduction of a transistor is not notable in Fig. 8, because the load current peak is approximately 30% lower than the load current peak shown in Fig. 9.

V. Conclusion

The laboratory setup of the half bridge inverter with the power section and control unit was developed in the Laboratory of Power Electronics. The power section presents the power module with two IGBTs and two freewheeling diodes. Inside of the control circuit there is the pulse-width modulator SG3525A, which outputs positive triggering pulses that are 180 degrees out of phase with an adjustable dead time interval between 0 and 22µs. These pulses are applied to the input of the hybrid dual driver SKHI22B, which outputs pulses for the transistor switching. The overall dead time in the output of the control unit is the sum of the dead times of the pulse-width modulator and hybrid dual driver. In this paper, the overall dead time is set to 3.9µs.

The validity of the simulation results was verified by the experiments carried out in the single-phase inverter laboratory setup. Through the analysed regimes and chosen parameters of the resistive-inductive load we noted very good agreement between the simulation and experiments results. The highest noted difference between the measured and simulated values of the load current is less than 5%, and the highest noted difference between the measured and simulated values of the load voltage is less than 10%. The difference in the load voltage was caused by the non-ideal DC voltage source.

In this paper, theoretical and experimental prerequisites for an analysis of voltage distortion effects caused by the dead time are made. This is one of the trends of modern research in the field of industrial electronics.

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