Strained Si/SiGe MOS transistor model

Tatjana Pešić-Brđanin, Nebojša Janković

Abstract— **In this paper we describe a new model of surface-channel strained-Si/SiGe MOSFET based on the extension of non-quasi-static (NQS) circuit model previously derived for bulk-Si devices. Basic equations of the NQS model have been modified to account for the new physical parameters of strained-Si and relaxed-SiGe layers. From the comparisons with measurements, it is shown that a modified NQS MOS including steady-state self heating can accurately predict DC characteristics of Strained Silicon MOSFETs.**

Index Terms—**Strained-Si, MOSFET, modeling.**

I. Introduction

Improvement in performance of Si MOSFETs through conventional device scaling has become more difficult, because of several physical limitations associated with the device miniaturization. [1]. Thus, much attention has recently been paid to the mobility enhancement technology through applying strain into CMOS channels [2-4]. Using Hall effect structures, high electron mobility have been measured in strained Si at room temperature and mobility approaching 500 000 cm /Vs has been demonstrated at 0.4 K [5]. Electron mobility enhancements in tensile-strained Si have been theoretically predicted for both bulk and inversion layer transport [6,7].

Strained-Si (SS) technology is emerging as a leading choise for continuous progression of transistor performances. For future circuit applications of these promising devices, the efficient SS MOSFETs modela are required. Consequently, there is a strong interest in the extension of conventional bulk SiMOSFET models to SS devices. A few studies of the extensions of the conventional bulk-Si MOSFET models published so far [8-10] have aimed primarily to estimate the implication of SS devices on final circuits performances. However, the validation of these models with experimental SS device data has not been presented.

In this paper, a new model of SS MOSFET is derived based on our recently described non-quasi-static bulk-Si devices model (the NQS MOS model) [11].

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It aapears that, owning to a small set of parameters directly related with the device underlining physics, the NQS MOS model can be easily modified to include new physical parameters of straines-Si and relaxed-SiGe layers. The modelling results of the modified NQS MOS model will be demonstrated by comparison with the experimental data of both SS NMOSFET and Si-control NMOSFET devices.

II. SS MOSFET

Fig. 1 shows a schematic illustration of the crystal lattice for strained Si on relaxed $Si_{1-x}Ge_x$, and the subsequent energy splitting of the Si conduction band edge. Because the equilibrium lattice constant of $Si_{1-x}Ge_x$ is larger than that of Si, a pseudomorphic layer of Si grown on relaxed $Si_{1-x}Ge_x$ is under biaxial tension. The strain lifts the sixfold degeneracy in the conduction band and lowers the two perpendicular valleys (labeled Δ_2 in Fig. 1) with respect to the four in-plane valleys (Δ_4). Electrons are expected to preferentially occupy the lower-energy Δ_2 valleys, reducing the effective in-plane transport mass. The energy splitting also suppresses intervalley phonon-carrier scattering, increasing the electron low-field mobility.

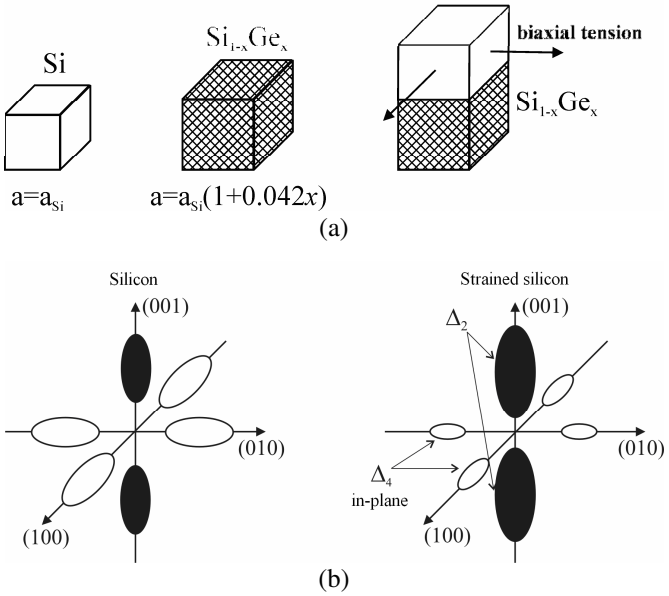


Fig. 1. Schematic illustrations of equilibrium lattice, peudomorphic strained Si on relaxed Si1-xGex (b) and strain-induced conduction band splitting in Si.

With the strained-Si layer pseudo-morphycally grown on the relaxed $Si_{1-x}Ge_x$ substrate ('virtual substrate'), the performance

of surface-channel MOSFETs can be greatly enhanced. The main benefit stems from the two effects, the improved carrier mobility and an increased electron saturation velocity. Besides the enhanced mobility, the other important physical parameters of SS and relaxed-SiGe layers (the energy band gap, the band offsets, the dielectric constants etc.) influence the SS MOSFET operation. Thus, compared to its bulk-Si counterpart, the SS NMOSFET exhibits a reduced threshold voltage and significantly higher self-heating effects (SHEs) [13-15].

A schematic cross-section of an experimental surface-channel SS NMOSFET fabricated on relaxed SiGe is shown in Fig. 2 together with its identical bulk-Si counterpart processed simultaneously on Si substrates. These test devices are used for parameters extraction and model validation.

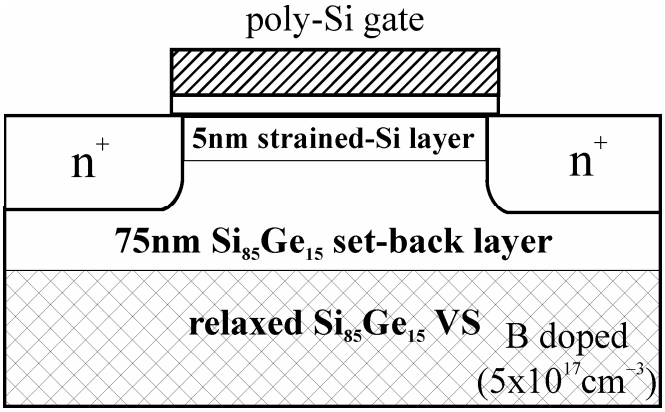


Fig. 2. Schematic cross-section of an experimental surface-channel SS MOSFET fabricated on relaxed $Si_{85}Ge_{15}$ virtual substrate.

Strained-Si n-channel MOSFETs were fabricated on relaxed SiGe virtual substrates with x=15%. The virtual substrates were grown by ultra low pressure CVD in a modified MBE system. A 16–nm strained-Si layer was grown on each virtual substrate, which resulted in a final strained-Si channel thickness of approximately 5 nm due to surface cleans and gate oxidation, as determined by transmission electron microscopy on fully processed devices.

Strained-Si–SiGe device fabrication followed a 0.25μm CMOS process. Active areas were defined in 400-nm deposited oxide, and a gate oxide was thermally grown at 800°C, resulting in a 6 nm gate oxide. Annealing in nitrogen at 800°C was subsequently carried out in order to reduce the gate oxide interface trap density. Polysilicon was deposited and devices down to 150 nm gate length were patterned using electron-beam lithography. As and P were implanted into the source, drain and gate through a thermally grown oxide and annealed at 1050°C for 20 s. Back-end processing comprised deposited silox and BPSG with Al metallization [14].

The modelling of strained-Si devices requires modification of the mobility model, energy band-gap model, as well as relative dielectric constant. Also, due to a poor thermal conductivity (at least fifteen times lower than that of Si of the thick SiGe underlayer) the self-heating effects have to be accounted in the modified NQS model.

III. Modeling the SS NMOSFETs

In order to extend the NQS MOS model [11] of bulk-Si devices on SS NMOSFETs, some of its basic formulas have to be upgraded to account for the new physics of SS and SiGe materials. Thus, new intrinsic carrier concentration ($n_{i,SS}$) and relative dielectric constant (ε_{SiGe}) of SS and SiGe layer, respectively, were introduced for calculating the Fermi potential (ϕ_f) and transistor body factor (γ) (see eqns. 3 and 4 in [11]). The band-gap dependence of Ge mole fraction (x) can be calculated from the widely accepted semi-empirical SS energy band-gap ($E_{g,SS}$) formula [16]:

$$E_{g,SS} = E_g - 0.4x = 1.11 - 0.4x \quad \text{(eV)} \tag{1}$$

The enhancement of low-field electron mobility in the SS layer is described by the new parameter $\mu_{dop,SS}$ that is related with the previous Si mobility parameter ($\mu_{dop,Si}$) by $\mu_{dop,SS} = m \cdot \mu_{dop,Si}$ The enhancement factor m was determined from the empirical mobility data of SS devices reported in [17], where, for example, $m \approx 1.6$ for x=0.15. Note that, in the case of the n-channel SS MOSFET, a single value of m is found to be a good approximation for both low and high gate voltage V_{GS} [17].

It is shown that the impact ionization is dominated in system strained Si/SiGe that silicon, due to band-gap narrowing. Eksperimentalno je pokazano da je udarna jonizacija veća u sistemu napregnuti Si/SiGe nego u slučaju čistog silicijuma pri istim uslovima spoljašnjih polarizacija, što je posledica smanjenja energetskog procepa napregnutog silicijuma. In NQS MOS model, the output drain current I_D in the pre-turn-on region can be expressed as [18]:

$$I_D = \frac{M}{1 - K(M-1)} I_{ch} \tag{2}$$

where I_{ch} is channel saturation current, obtained by NQS MOS sub-circuit, K is the pre-turn-on slope factor. The following **empirical** expression of K versus the effective channel length L_{eff} for SS MOSFET is found $K = k_1 L_{eff}^{k_2}$ (paremeters k_1 and k_2 are given in Table I); M is the well-known avalanche multiplication factor [19]:

$$M = 1 + \frac{A_n l_d E_m}{B_n} \exp\left(-\frac{B_n}{E_m}\right) \tag{3}$$

where:

TABLE I
THE NQS MOS MODEL PARAMETERS OF BULK-SI AND STRAINED-SI/SIGE NMOS TRANSISTORS

Param.	Description	Si MOS	SS MOS
L_{eff}	Channel lenght (μm)	0.1, 0.2, 9.9	0.1, 0.2, 9.9
W	Channel width (μm)	5	5
ΔL	Drain/source – gate overlap length (μm)	0.05	0.05
t_{ox}	Gate oxide thickness (nm)	6	6
x_j	Junction depth (μm)	0.1	0.1
V_{fb}	Flatband voltage (V)	-0.68	-0.94
N_{beff}	Effective channel doping (cm^{-3})	$5\cdot10^{17}$	$2.9\cdot10^{17}$
μ_{dop}	Doping dependent low-field mobility (cm^2/Vs)	280	476
α	Vertical field mobility degradation factor (V^{-1})	0.33	0.37
v_{sat}	Saturation velocity (cm/s)	$1.206\cdot10^7$	$2.29\cdot10^7$
β_0	Lateral mobility fitting parametet	1.109	1.109
R_S, R_D	Sorce/Drain resistance (Ω)	140	200
DIBLL	Pre-factor for length dependence of DIBL effect	0.00102	0.000812
DIBLE	Exponent for length dependence of DIBL effect	-2.1	-1.56
VFBLL	Pre-factor for length dependence of flatband voltage (V)	-0.346	-1.08
VFBLE	Exponent for length dependence of flatband voltage (V)	-0.42	0.1
CSLL	Pre-factor for length dependence of body effect	0.46	0.942
CSLE	Exponent for length dependence of body effect	-0.6	-0.105
C	Pre-factor for channel length modulation effect	0.042	0.06
D	Exponent for channel length modulation effect	0.5	0.5
k_1	Pre-factor for K dependence	0.47	0.39
k_2	Exponent for K dependence	-0.43	-0.25
A_n	Impact ionization parameter	$2.45\cdot10^5$	$2.84\cdot10^5$
B_n	Impact ionization parameter	$1.92\cdot10^6$	$3.64\cdot10^6$
t_1	Pre-factor for self-heating effect	–	0.045
t_2	Exponent for self-heating effect	–	0.6

$$l_d = 1.7\cdot10^{-2} t_{ox}^{1/8} x_j^{1/3} L_{eff}^{1/5} \tag{4}$$

x_j is pn juntion depth, while A_n and B_n are impact ionization parameters. In eqn. (3), E_m is maximal channel electric field depending of drain voltage V_{DS} as:

$$E_m = \sqrt{\frac{V_{DS}^2}{l_d^2} + \frac{2E_a V_{DS}}{l_d}} \tag{5}$$

where E_a include gate voltage V_{GB} and source surface potential ϕ_{S1} dependences:

$$E_a = \frac{qN_B l_d}{\varepsilon_0 \varepsilon_{Si}} - \frac{\left(V_{GB} - V_{fb} - \phi_{S1}\right)}{l_d} \tag{6}$$

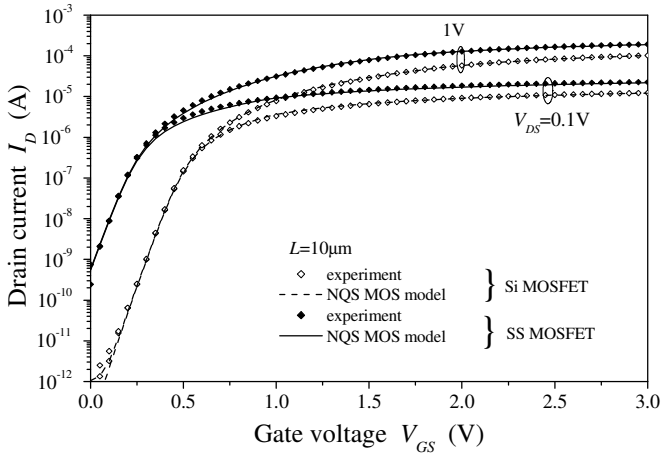
The parameter values with notation and meanings are shown in Table I. They were extracted in the same way as for the case of modelling the bulk-Si devises described in details in [11].

The method of SS NMOSFET model parameter's extraction is identical as in the case of modeling bulk-Si devices [11]. The process-related parameters including effective gate length (L_{eff}), oxide thickness (t_{ox}), and the effective channel doping (N_{beff}) were known from device geometry and processing. The other parameters, more related with device physics, were found from tuning the simulated and the measured electrical characteristics of several SS devices with various channel lengths. The flat-band voltage parameter (V_{fb}) was extracted from matching the experimental transfer characteristics $I_D - V_{GS}\big|_{V_{DS}=const}$ of the long-channel devices in the sub-threshold region. A theoretical values of velocity saturation parameter (v_{sat}) and the corresponding exponent (β_0), both appearing in the transverse field dependence MOS mobility model, were fine tuned until good match with experimental $I_D - V_{DS}$ output characteristics of short-channel devices around saturation ($V_{DS} \sim V_{Dsat}$) was achieved at high V_{GS}. Namely, in this region, the saturation of output characteristics of short-channel transistors is governed by v_{sat} and not the pinch-off of channel charge. The parameter α, figuring in lateral field dependence mobility models, was evaluated from long-channel $I_D - V_{DS}$ experimental characteristics, aiming to avoid the interference of short-channel effects on the decrease of output conductance. Due to the dominance in short-channel devices, the source/drain ohmic resistances (R_D, R_S) were evaluated from the linear region of $I_D - V_{DS}$

characteristics of short-channel devices. Finally, the only true fitting parameters *DIBLL*, *DIBLE*, *VFBLL*, *VFBLE*, *CSLL* and *CSLE* describing short-channel effects [11] were found from the sub-threshold region of $I_D - V_{GS}$ transfer characteristics of short-channel devices, until a good match was achieved for both low and high constant V_{DS} .

IV. RESULTS

The simulated and the measured transfer and output characteristics of otherwise identical SS MO SFET on 15% Ge virtual substrate and bulk-Si devices with different channel lengths are shown in Figs. 3-5. The characteristics are obtained with using a unified set of NQS MOS model parameters (shown in the table I) for modelling each of the experimental devices.



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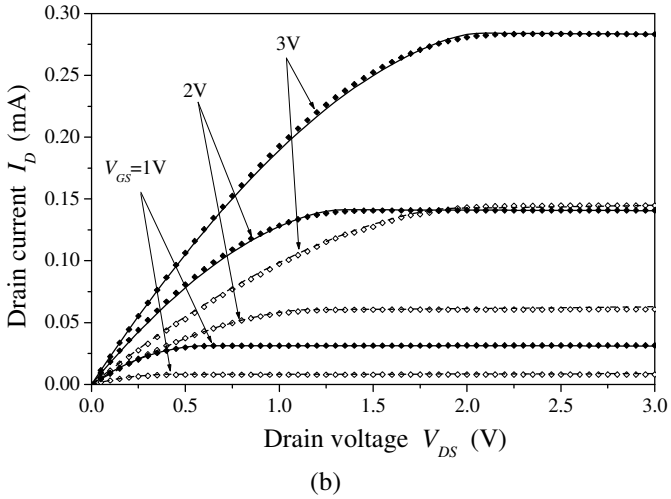
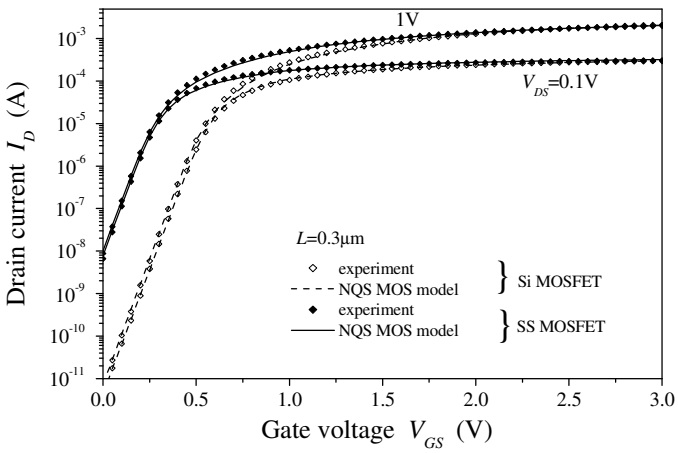


(b)

Fig. 3. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 10\mu m$.



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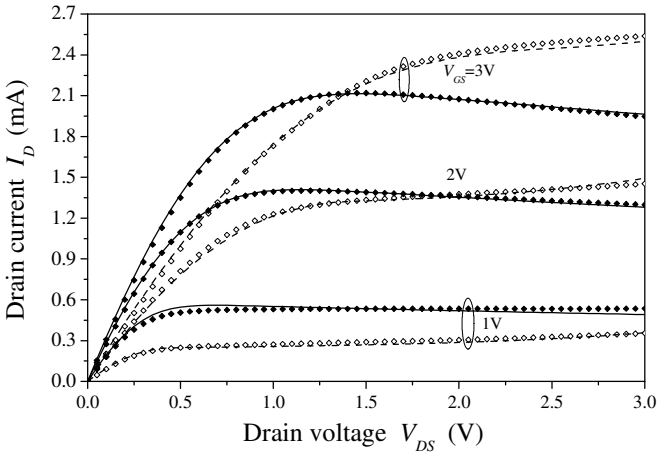
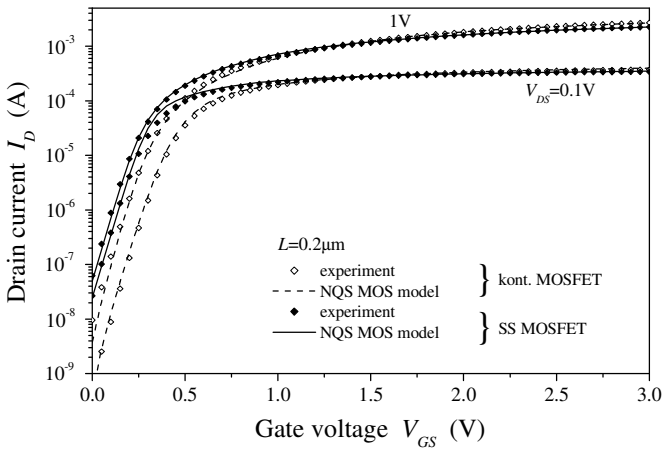


(b)

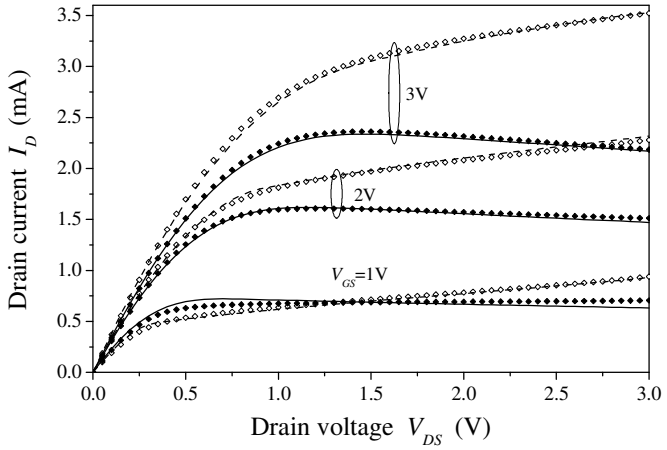
Fig. 4. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 0.3\mu m$.

The DC (or steady-state) self-heating phenomena of MOS devices refer to local increase of channel temperature with dissipating power, that in turn limits maximum device current drive performance. The three main SHEs in NMOSFETS are: a decrease of channel mobility, a drop of threshold voltage and an increase of carrier's saturation velocity. In the higher power dissipative region, however, the mobility degradation predominates all other effects, which subsequently appears as a negative conductance in device output characteristics. SHEs have been incorporated in SS device model through its phenomenological dependence on V_{DS} . Assuming that all SHEs can be summed into one lumped effect of channel mobility degradation, a modified low-field mobility parameter is defined as $\mu^*_{dop,SS} = \mu_{dop,SS} \cdot (1 - t_1 \cdot V_{DS}^{t_2} \cdot L_{eff}^{-1})$, where parameters t_1 and t_2 are given in Table I. From Fig. 4 and Fig. 5, it is seen that the negative output conductance is highly visual in short-channel SS NMOSFETs, whereas the same is not observed in the control Si transistors. However, it is not appeared yet in long-channel SS device characteristics of Fig. 3 due to a substantially lower power dissipation for given

V_{GS}, V_{DS} and because of smaller R_{th} in larger transistors ($R_{th} \sim L^{-1}$). Consequently, since $\mu^{*}_{dop,SS}$ is less degraded, a current drive enhancement of the SS device over its bulk-Si counterpart is clearly visible for long-channel transistors as shown in Fig. 3. In case of short channel transistors, however, the potential advantage of SS devices is masked by negative conductance and can be revealed in simulations by omitting the SHE model.



(a)



(b)

Fig. 5. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 0.2\mu m$.

V. CONCLUSION

The bulk-Si NQS MOS device model was successfully modified and implemented for modelling DC characteristics of surface-channel strained-Si NMOSFEs. An efficient method for including the steady-state self-heating effects in the NQS MOS model, which avoids the conventional method of the device temperature extractions with auxiliary subcircuits is also described. From the comparisons of modelling results with numerical simulations and measurements, it is shown that a modified NQS MOS including steady-state self-heating can accurately predict the DC characteristics of strained-Si/SiGe NMOSFETs. It can be also useful for extracting sound physical values of all other model parameters and for realistic estimation of channel mobility enhancement in SS devices beiing marked by the loss of current drive performance due to SHEs.

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