ELECTRONICS

Editorial

THE most of the content in this issue of Electronics journal is dedicated to VII symposium of Industrial Electronics – INDEL 2008. Symposium is held on 7th to 8th November 2008. at Faculty of Electrical Engineering in Banjaluka. Chairmen's of all sections have suggested the best paper of each section for this issue of Electronics journal.

Invited paper "Preliminary Design of a PEM Fuel Cell Simulator Based on Digitally Controlled DC-DC Buck Converter" of authors G. Georgievski and G. Arsov presents model for a PEM fuel cell that can be used to design fuel cell simulator. The model is consisted of a DC-DC buck converter driven by PIC16F877 microcontroller.

The paper "Statistical Timing Analysis of Asynchronous Circuits Using Logic Simulator" of authors M. Sokolović and V. Litovski describes a method for statistical estimation of topological delays in asynchronous circuits, based on the application of a VHDL simulator.

New model of surface-channel strained-Si/SiGe MOS transistor is described in paper "Strained Si/SiGe MOS transistor model" of authors T. Pešić-Brđanin and N. Janković. It is shown that a modified NQS MOS model can accurately predict DC characteristics of Strained Silicon MOSFETs.

In paper "Power Quality Monitoring and Power Measurements by Using Virtual Instrumentation" of authors Z. Kokoloanski and others is described a virtual instrument used for monitoring and analysis of the relevant power quality parameters, load control and power measurements.

The paper "Influence of Imperfect Carrier Signal Recovery on Performance of SC Receiver of BPSK Signals Transmitted over α-μ Fading Channel" of authors Z. Mitrović and others presents the analysis of the reception of binary phase-shift keying signals transmitted over the generalized α-μ fading channel.

Authors A. Rakić and T. Petrović have shown in their paper "Multivariable Modeling and Decentralized Robust Linear Controllers for Current-Sharing DC/DC Converters" that proposed multivariable linear models are suited for frequency framework of various linear control design techniques.

Regular paper "A Thyristor Full-Wave Rectifier With Full Control of the Conducting Angle" of author R. Stevanović describes the full-wave thyristor rectifier with two cells ladder RC network for control of the conducting angle.

Branko Dokić Ph.D.

Preliminary Design of a PEM Fuel Cell Simulator Based on Digitally Controlled DC-DC Buck Converter

Goce L. Arsov, Georgi Georgievski

Abstract—**Modeling of fuel cells is getting more and more important as power fuel cell stacks being available and have to be integrated into real power systems. This paper presents a novel circuit model for a PEM fuel cell that can be used to design fuel cell simulator. The model is consisted of a DC-DC buck converter driven by PIC 16F877 microcontroller. The model can be used in design and analysis of fuel cell power systems by simulation or by using practically realized simulator.**

Index Terms—**PEM Fuel cell, Modeling, Simulation, Pulse Width Modulation (PWM).**

I. INTRODUCTION

FUEL cells as energy source have been present since 1839. They were discovered and developed by the English physicist William Grove. But, since then, for more over one century they were not more than a laboratory curiosity [1]. After the period of 120 years since the fuel cells emerged, NASA demonstrated some of their potential applications in the space flights exploration. Consequently, the industry has started recognizing the commercial aspects of the fuel cells, which, due to the technological barriers and their high production costs, were not economically profitable at that stage of technology [2].

Today, fuel cells of various types have emerged as promising alternative sources of "clean energy" for applications ranging from automotive industry to residential and commercial installations. This has created a need for a class of specialized power converters geared to interface between the fuel cell device and the end-user appliance, often as a battery charger. Specifications for power conversion equipment depend on the fuel cell's physical properties and manufacturing economics.

The most common application areas of fuel cell can be classified in five main groups as shown in Fig. 1 [3].

The cells' output voltage is dependent on the load. So, there is a need to model the fuel cell for optimizing its performance and also for developing fuel cell power converters for various
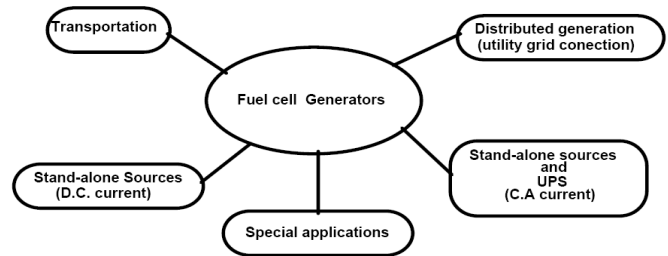
Fig. 1. Classification of fuel cell application.

applications.

The proton exchange membrane fuel cell (PEMFC) has been considered as a promising kind of fuel cell during the last 20 years because of its low working temperature, compactness, and easy and safe operational modes. The proton exchange membrane (PEM) fuel cell is very simple and uses a polymer (membrane) as the solid electrolyte and a platinum catalyst.

A fuel cell stack is composed of several fuel cells connected in series separated by bipolar plates and provides fairly large power at higher voltage and current levels.

Up to now different type of models of PEM fuel cell were proposed $[4]-[12]$. Unfortunately, most of the proposed models cannot be used for practical realization of a fuel cell simulator.

The aim of this paper is to propose a model of a PEM fuel cell which can be extended to a practical realization of a fuel cell simulator that can be used in preliminary design of fuel cell based systems.

II. DESCRIPTION AND OPERATIONAL PRINCIPLE OF THE FUEL CELLS

The fuel cell is a mini power source generating electrical energy without the combustion stage. The basic physical structure, or building block, of a fuel cell consists of an electrolyte layer in contact with a porous anode and cathode on either side [13]. Porosity of the electrodes enhance the active electrode area hundreds, even thousand times. This fact is very important because electrochemical reactions take place on the electrode surface. Catalyst is incorporated in the electrode microstructure, e.g., platinum, nickel or their alloys which accelerate the speed of electrode's electrochemical reactions

[13]. The chemical energy is directly transformed into electrical energy and heat when the hydrogen fuel reacts with the oxygen from the air [14], [15]. Water is the sole byproduct of the reaction. The basic electrochemical reaction is the following one [16]:

Anode reaction: $H_2 \rightarrow 2H^+ + 2e^-$ (1)

Cathode reaction: $\frac{1}{2}O_2 + 2H^+ + 2e^- \rightarrow H_2O$ (2)

Overall reaction: $\frac{1}{2}O_2 + H_2 \rightarrow H_2O$ (3)
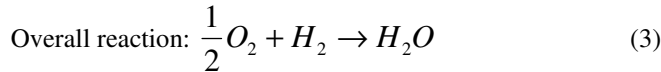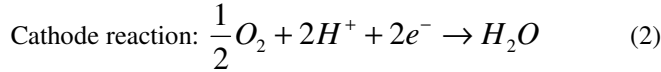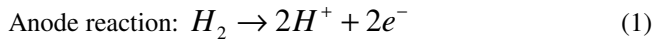
Looking at the the previous equations, one can get a wrong impression that this process is very simple, but actually the physical and chemical processes happening on each of the electrodes and membrane are rather complex. A schematic fuel cell representation with flow directions of the fuel, reactant and ion current is given in the Fig. 2 [17].

Single fuel cell at no load (e.g. polymere electrolyte fuel cell - PEFC) in ideal case, generates voltage of 1,16 V at the temperature of 80 °C and gas pressure of 1 bar. Loaded fuel

Fig. 2. Operational principle of the fuel cell.

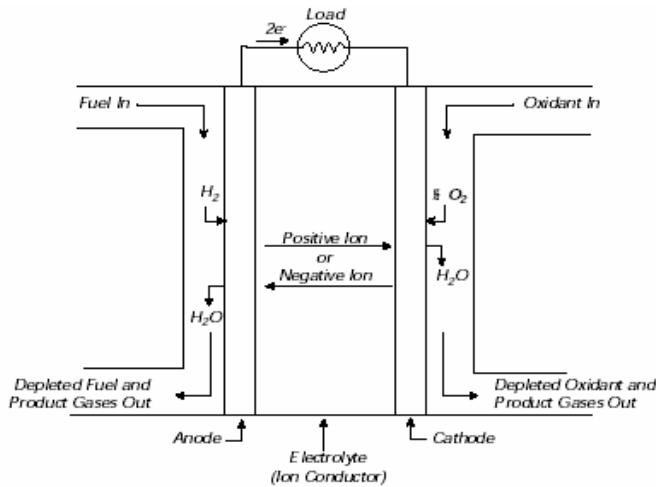cell at this operational conditions generates 0,7 V. Thereby 60% of the fuel energy is transformed into electrical energy [14]. Maximum emf, E, gained during the hydrogen and air reaction (H_2 + ½$O_2 \rightarrow H_2O$) at the specified values of temperature and pressure can be determined by the following expression:

$$E = -\frac{\Delta g_f}{nF}$$ (4)

where Δg_f is Gibbs free energy, n is number of electrons participating in the reaction, and F is the Faraday constant.

In order to use the fuel cell as energy source practically, a number of single fuel cell has to be serially connected (stacked) to gain the higher output voltage.

When the hydrogen is used as a fuel, the pollutants are not products of the reaction. Hydrogen fuel could be produced by electrolysis process using renewable power sources as sun, hydro, geothermal and wind energy. But the hydrogen could be extracted from any hydrocarbons e.g. petrol, naphta,

biomass, natural and LPG, methanol, ethanol, etc.

The most often classification of the fuel cell is according to the type of the used electrolyte [13]. So there are five types of fuel cell although basically the same electrochemical reaction takes place in all of them [13]:

- Alkaline Fuel Cell - AFC： AFC operating at 250 °C has an electrolyte of highly concentrated potassium hydroxide KOH while those operating at lower temperatures (120 °C) have lowly concentrated KOH. The electrolyte is retained in an asbestos matrix. Wide spectrum of catalysts is used: Ni, Ag etc. The fuel is limited to non-reactive constituents except for hydrogen.

- Polymer Electrolyte Membrane Fuel Cell - PEMFC: Electrolyte in this fuel cell is ionic membrane (Sulfuric acid polymer) which is excellent ionic conductor. Water is the only liquid in the PEMFC and consequently the problem with the corrosion of PEMFC elements are minimal. Water management is a key factor for PEMFC efficient operation. During the operation the PEMFC the humidity of the membrane is critical which determines the operational temperature of the PEMFC in the range of 60-100 °C. The fuel is hydrogen H_2 enriched gas with no presence of CO (fuel cell poison at low temperatures). Platinum is used as a catalyst

- Phosphoric Acid Fuel Cell - PAFC： Concentrated phosphoric acid (up to100%) is used in PAFC at operating temperatures in the range of 150 - 250 °C. At lower temperatures, phosphoric acid is bad ionic conductor, and catalyst (Pt) poisoning with CO becomes extremely severe. The relative stability of the phosphoric acid is high compared to the other acids, and that is the reason why this acid is operative at high temperatures with small water quantity which make the water management easy. Electrolyte is put up in silicon matrix while the type of the used catalyst is Pt.

- Molten Carbonate Fuel Cell - MCFC: MCFC's electrolyte is combination of alkali carbonates or combination of Na and K, placed in a ceramic matrix made up of $LiALO_2$. Operational temperature of the MCFC is in the range of 600 °C to 700 °C at which the alkali carbonates form highly ionian conductive molten salt. Ni (anode) and nickel oxide (cathode) are used to promote reaction.

- Solid Oxide Fuel Cell - SOFC: The memebrane electrolyte is solid nonporous metalic oxide usually Y_2O_3 - stabilized ZrO_2. Operational temperature is in the range from 650 to 1000 °C where ionic conduction of oxygen ions occurs. Typically anode is made of $Co-ZrO_2$ or $Ni-ZrO_2$ cermet and cathode is Sr-doped $LaMnO_3$.

Initial use of the fuel cells was in the NASA's space flights, for power generation and production of fresh water for the astronauts. Today the fuel cells might be used in three categories of aplications: transport, stationary and portable aplications.

AFC is the first modern type of fuel cell developed in the 1960's for the "Apollo" space program. The excellent performances of AFC comparing to the other types of fuel

cells, are due to the active O_2 electrode kinetics and its flexibility to use a wide range of elctrocatalysts. But, pure H_2 has to be used as fuel because CO_2 in any reformed fuel reacts with KOH electrolyte to form carbonate thus reducing the electrolyte's ion mobility. Purification of the fuel is rather expensive and because of that the use of AFC is limited to the space applications where fuel is pure hydrogen. In the NASA's Space shuttle three 12 kW units have been used for 87 missions with 65 000 hours flight time duration.

PEMFC are used in the transport aplications. Exceptionally interesting for this kind of applications is the Direct Methanol Fuel Cell - DMFC. In this type of fuel cell metilacohol (methanol) is directly used as a fuel needing no reformer stage [14]. PEMFC generate electrical energy with high efficiency and power density (180 - 250 mW/cm2) [13]. Also, this type of fuel cells can be used in a small stationary applications for generation of electrical power and heating in the individual houses. The power range is from 2 to 10 kW. This achievement is made by the cost reduction of the materials and manufacturing. Their main advantage is low operating temeperatures 60-100 °C and solid electrolyte. Due to the low operational temperature anode catalyst poisoning with CO is significant especially at higher current densities. In this case the output voltage of the fuel cell becomes unstable and fluctuating. Also due to the low operating temperatures, expensive catalysts have to be used for increasing the speed of the electrochemical reactions (platinum).

PAFC are for the time being the only one commercialized type of the fuel cell. It is relatively simple, reliable and quiet power source with 60% efficiency (with cogeneration). As fuel could be used natural gas. 60 MW of this type fuel cells generators are installed worldwide. The power range of the most of the power stations is between 50 and 200 kW, but also they are constructed in the range between 1 and 5 MW. Operational temperature is around 200 °C, and power density reaches values of 310 mW/cm². The PAFC anode is very sensitive to catalyst poisoning even if very small concentrations of contaminants (CO, COS and H_2S) are present. Compromise between the demand for high power density and good operational performances through the life spans of the PAFC should be made. One of the primary targets for the future PAFC development is the extension of the PAFC's life span up to 40 000 hours.

MCFC operates at around 600 °C. At this temperature many of the disadvantages of the lower as well as higher temperature cells can be alleviated with the fact that, for manufacturing MCFC, commonly available materials can be used (utilization of metal sheets reduces fabrication costs), while nickel catalyst is used instead of expensive precious metals. Reforming process takes place within the cell and CO is used directly as a fuel. However, the electrolyte in the MCFC is very corrosive and mobile while the higher temperature influences the mechanical stability and the lifetime of the MCFC materials. An Energy Research Corporation (ERC) in USA has tested a 2MW power supply which operates from 1996 in Santa Clara, Ca.

SOFC electrolyte is solid and cell can be made in tubular, planar or monolithic shape. The solid ceramic construction of the cell alleviates hardware corrosion problems characterized by the liquid electrolyte cells and is impervious to gas cross-over from one electrode to the other. The absence of liquid also eliminates the problem of electrolyte movement and flooding the electrodes. The kinetics is fast while CO is directly usable fuel as in MCFC. Also, as in MCFC, there is no requirement for CO_2 at the cathode. Operational temperature is around 1000 °C which means that the fuel is directly reformed within the cell. Disadvantages of the high operational temperature are the influences on the cell's material properties meaning the different thermal expansion mismatches. Currently two plants (25 kW and 100 kW), produced by Siemens Westinghouse Power Corporation, are installed and they both have cumulative operating time of 9500 hours. The eventual SOFC market is for large stationary fuel cell power supply systems (100 to 300 MW) using natural gas or coal as a fuel.

III. FUEL CELL CHARACTERISTICS [13], [17], [18]

The fuel cell directly converts chemical energy into electrical energy. The chemical energy released from the fuel cell can be calculated from the change in Gibbs free energy (Δ_{gf}) which is the difference between the Gibbs free energy of the product and the Gibbs free energy of the reactants [18]. The Gibbs free energy is used to represent the available energy to do external work. For the hydrogen/oxygen fuel cell, the basic chemical reaction is given by (3), and the change in the Gibbs free energy can be expressed as:

$$\Delta g_f = g_{f.of.products} - g_{f.of.reac\tan ts}$$

$$= (g_f)_{H_2O} - (g_f)_{H_2} - (g_f)_{O_2} \qquad (5)$$

The change in Gibbs free energy varies with both, temperature and pressure:

$$\Delta g_f = \Delta g_f^{\;o} - RT_{fc}\, ln\left[\frac{p_{H_2}\, p_{O_2}^{\;1/2}}{p_{H_2O}}\right] \qquad (6)$$

where $\Delta g_f^{\;o}$ is the change in Gibbs free energy in standard pressure (1 bar) which varies with temperature T_{fc} in Kelvin. The partial pressures p_{H2}, p_{O2} and p_{H2O} of the hydrogen, oxygen and vapor are expressed in *bar*. *R* is the universal gas constant, 8.31454 J/(kg·K). The value of Δg_f is negative, which means that the energy is released from the reaction.

For each mole of hydrogen, two moles of electrons pass around the external circuit and the electrical work done (charge × voltage) is:

$$W = -2FE \quad \text{(J)} \qquad (7)$$

where *F* is the Faraday constant (96485 C) which represents the electric charge of one mole of electrons and *E* is the voltage of the fuel cell. The electrical work done would be

equal to the change in Gibbs free energy if the system were considered reversible. Now, the equation (4) can be rewritten as:

$$\Delta g_f = -2FE \qquad (8)$$

The reversible open circuit voltage of the fuel cell or "Nertst" voltage of hydrogen fuel cell is [18]:

$$E = -\frac{\Delta g_f}{2F} = \frac{\Delta g_f^o}{2F} + \frac{RT_{fc}}{2F} ln\left[\frac{p_{H_2} p_{O_2}^{1/2}}{p_{H_2O}}\right] \qquad (9)$$

$$E = 1.229 - 0.85 \times 10^{-3}(T_{fc} - 298.15) +$$

$$+ 4.3085 \times 10^{-3} T_{fc}\left[\ln(p_{H_2}) + \frac{1}{2}\ln(p_{O_2})\right] \qquad (10)$$

T_{fc} is expressed in Kelvin, and p_{H2} and p_{O2} in atm.

The actual voltage of the fuel cell is less than the value calculated by equation (10). Typical PEM fuel cell performance plot is given in Fig. 3. The differences are result of losses or irreversibilities.

The current density, cell current per cell active area $A_{fc}(cm^2)$, is:

$$i = \frac{I_{st}}{A_{fc}} \qquad (11)$$

The fuel cell losses are attributed to three categories: the *activation* loss, the *ohmic* loss and the *concentration* loss.

The voltage drop due to activation loss is dominated by the cathode reaction conditions. The relation between the activation overvoltage v_{act} and the current density is described by the Tafel equation:

$$v_{act} = a\,ln(\frac{i}{i_0}) \qquad (12)$$

where, a is a constant and i_0, the exchange current density, is also a constant. Both constants can be determined empirically. For low temperature PEM fuel cell, the typical value of i_0 is about 0.1mA/cm^2.

The ohmic loss arises from the resistance of the polymer membrane to the transfer of protons and the resistance of the electrode and the collector plate to the transfer of electrons. The voltage drop that corresponds to the ohmic loss is proportional to the current density:

$$v_{ohm} = i \cdot R_{ohm} \qquad (13)$$

R_{ohm} ($\Omega \cdot cm^2$) is the internal electrical resistance. The resistance depends strongly on the membrane humidity and the cell temperature.

The concentration loss or concentration overvoltage results from the drop in concentration of the reactants as they are consumed in the reaction. These losses are the reason for rapid voltage drop at high current densities. The voltage drop due to concentration losses is given by:

$$v_{conc} = i(c_2 \frac{i}{i_{max}})^{C_3} \qquad (14)$$

where c_2, c_3 and i_{max} are constants that depend on the temperature and the reactant partial pressure and can be determined empirically. The parameter i_{max} is the current density that causes precipitation voltage drops.
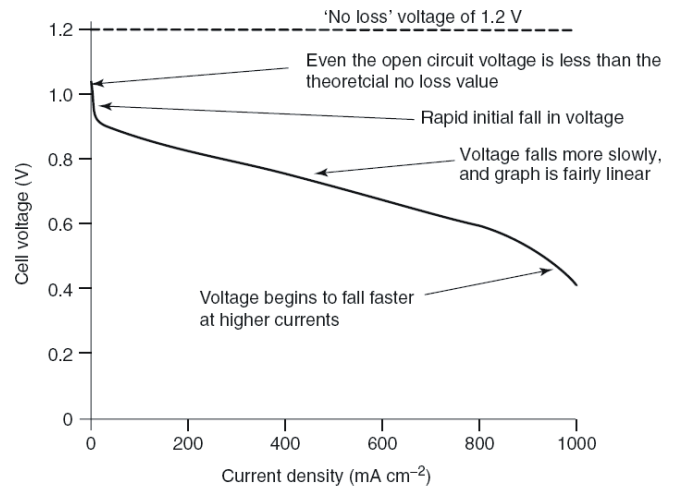
Fig. 3. Graph showing the voltage-current dependence of a typical PEM fuel cell.

By combining all voltage drops associated with all the losses, the single fuel cell operating voltage can be written as:

$$v_{fc} = E - v_{act} - v_{ohm} - v_{conc} =$$

$$= E - aln(\frac{i}{i_0}) - [iR_{ohm}] - \left[i\left(c_2\frac{i}{i_{max}}\right)^{C_3}\right] \qquad (15)$$

where, the open circuit voltage E is given by (10).

The fuel cell stack comprises multiple fuel cells connected in series. The stack voltage can be calculated as:

$$v_{st} = nv_{fc} \qquad (16)$$

IV.   CIRCUIT MODEL OF A PEM FUEL CELL SIMULATOR

The circuit diagram for simulating the fuel cell characteristics, which can be realized for experimental investigations, is composed of two parts: the power circuit and the control circuit.

To achieve appropriate power supplied to the load, the DC-DC buck converter has been proposed as a main power circuit. The microcontroller PIC 16F877 [19] is used to implement the proper fuel cell $\tilde{V}I$ characteristics into the DC-DC converter.

The complete circuit is shown in Fig. 4.

Fig. 4. Proposed circuit model of PEM fuel cell module.

A. Design of the DC-DC buck converter

The main stage of the proposed circuit consists of a classical buck converter shown in Fig. 5.
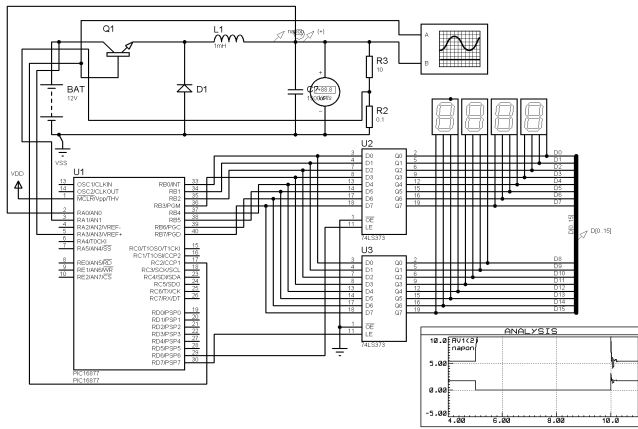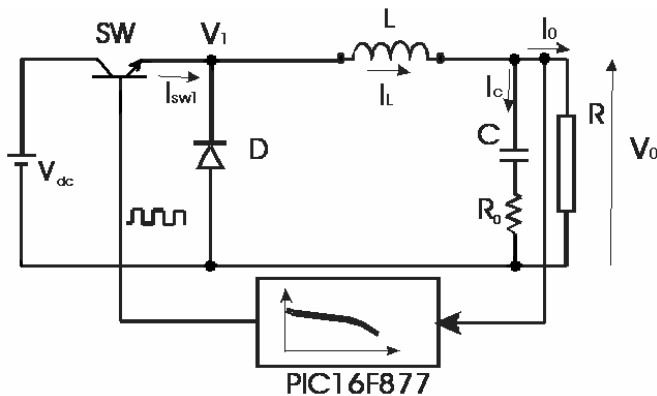

Fig. 5. DC-DC buck converter.

The design procedure of the buck converter is based on the methodology explained in [20].

In general, the output voltage of the buck converter can be defined as $V_0 = V_{dc}T_{on}/T$, where T_{on} is the interval during which the switch is ON, and is independent of whatever the switching period T is [20]. The question arises as to whether there is an optimum period and on what basis the period is selected.

The switching losses are proportional to the switching time of the transistor, τ, as shown by (17). The switching time is defined by the turn-on and turn-off intervals during one period

of the control signal. Decreasing T results in increased losses and possible necessity for use of large heat sink to keep the switching transistor temperature within desired limits.

$$P_{sw} = \frac{V_{dc}I_o}{2}\frac{\tau}{T} \qquad (17)$$

In order to use higher switching frequencies the diode, D, should be specified as ultra fast recovery type, which has reverse recovery time as low as 35 to 50 ns. Thus, the increasing of the switching frequency will decrease the size of the filter elements, L and C, but will contribute to the total losses and to the requirement for a larger heat sink. Optimum switching frequency for this type of circuits is found to be between 25 and 50 kHz.

The values of the inductance L and the capacitance C may be chosen in the following manner.

The value of the inductance L is usually specified in the manner that it's current does not become discontinuous before the DC output current falls to its specified minimum value, which in most cases is one-tenth of the nominal value, or $0.1 \times I_{on}$.
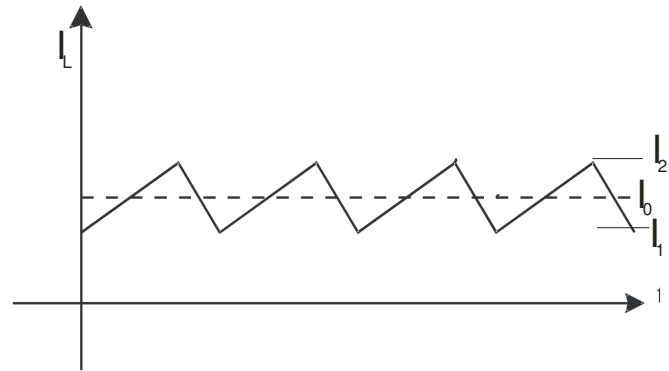
Fig. 6. Inductor current I_L.

The onset of the discontinuous mode occurs at a DC current equal to half the amplitude of the inductor current ramp. For $V_{dc} = 12$V, $I_{on} = 5$A, $T = 40 \times 10^{-6}$s, and $V_0/V_{dc} = 0.5$, the inductor L is:

$$L = \frac{(V_{dc}-V_0)T_{on}}{dI} = \frac{(V_{dc}-V_0)T_{on}}{0.2 \cdot I_{on}} \qquad (18)$$

$$T_{on} = V_0 T / V_{dc} \qquad (19)$$

$$L = \frac{5(V_{dcn}-V_0)V_0T}{V_{dcn}I_{on}} = 120\mu H \qquad (20)$$

where, V_{dcn} and I_{on} are their nominal values. The inductor must be designed so that it does not saturate at DC current of $1.1I_{on}$. The selected inductor can tolerate higher output currents, than the specified I_{on}, if the used core is designed not to enter the saturation region at these higher currents. The only restrictions on maximum currents in the buck converter are the increased

DC and switching losses in the switching transistor.

The value of the capacitance C is chosen to meet the output voltage ripple specifications. It is not an ideal capacitor. A real capacitor has the parasitic resistance R_0 and inductance L_0 in series with its capacitance. These are referred to as the equivalent series resistance (*ESR*) and equivalent series inductance (*ESL*). Below 300 kHz, L_0 can be neglected and output ripple is determined by R_0 and C. There are two ripple components, due to C and R_0. The ripple component due to *ESR* is proportional to the (I_2-I_1), the peak to peak inductor ramp current, as shown in Fig. 6. The ripple component due to C is proportional to the average current value. For the most frequently used types (aluminum electrolytic capacitors) over a large range of voltage ratings and capacitance values, the product R_0C tends to be constant. Usually, its range is from $(50-80) \times 10^{-6}$. Let's assume that the resistive ripple component V_{rr} is 0.05V peak to peak. Then, we may write down: $V_{rr} = 0.05 = (I_2-I_1)R_0$, or, for $I_2 - I_1 = 1$ A, we will obtain $R_0 = 0.05$ Ω. Now, for $R_0C = 50 \cdot 10^{-6}$:

$$C = 50 \cdot 10^{-6}/0.05 = 1000 \mu F \qquad (21)$$

The capacitive ripple voltage V_{cr} is produced from the average value of current $(I_2-I_1)/4 = 0.25$A. This current produces a ripple voltage across C described by (22):

$$V_{cr} = \frac{\Delta I \cdot t}{C} = \frac{0.25 \cdot 40 \cdot 10^{-6}}{1000 \cdot 10^{-6}} = 0.01 \text{ V} \qquad (22)$$

The total peak to peak capacitive ripple voltage is 0.01V. This may be ignored, compared with the ripple voltage as a result of R_0.

The calculation of L and C, as well as the selection of the bipolar transistor and the diode, should be reconsidered for any different case, depending on the voltage and current capabilities of the simulated fuel cell. For simulation purposes this can be done by the software but when using hardware solution this components should be physically changed.

B. The control algorithm

The microcontroller PIC16F877 is proposed for controlling the proper work of the power stage. In general, this is a "computer on a chip" that can be programmed and reprogrammed by the end user.

The PIC16F877 includes 10-bit multi-channel Analog-to-Digital converters and two PWM modules by which pulse width modulation can be easily implemented. The Analog-to-Digital converter is used to convert the analog values of the output voltage and current into digital for further processing. Using 10-bit A/D converter, the discretization error will be less than 0.1%. For example, if the ideal no load voltage is selected to be $V_{dc} = 12$ V, the discretization error will be less than 0.01 V. The PIC16F877 can be easily programmed using its instruction set consisted of 35 instructions. The instruction cycle of 200 ns allows us very good real time operation.

Although the simulated curve can be calculated using relations $(8) - (16)$, or by using some of the referred simulation models, here we use the measured polarization curve, of a single fuel cell, at specified conditions which is implemented in the PIC memory. The values can be modified depending of the stack current and voltage capabilities, as well as the working temperature.

In this case we have implemented the polarization curve for a single PEM fuel cell with "no loss" voltage of 1.2V and maximum current 1A, according to the Fig. 3. The working temperature is assumed to be 80 °C, and the pressure is standard (100 kPa).

The control algorithm is shown with its block diagram in Fig. 7. The actual output current, $I_{0(t)}$, and voltage, $V_{0(t)}$, are converted to 10-bit digital numbers using the A/D module. After comparison with previous values and with the values defined by the implemented polarization the command sequence for driving the PWM module is generated. Now the PWM module generates pulses for proper driving of the switching transistor thus controlling the output voltage V_0.
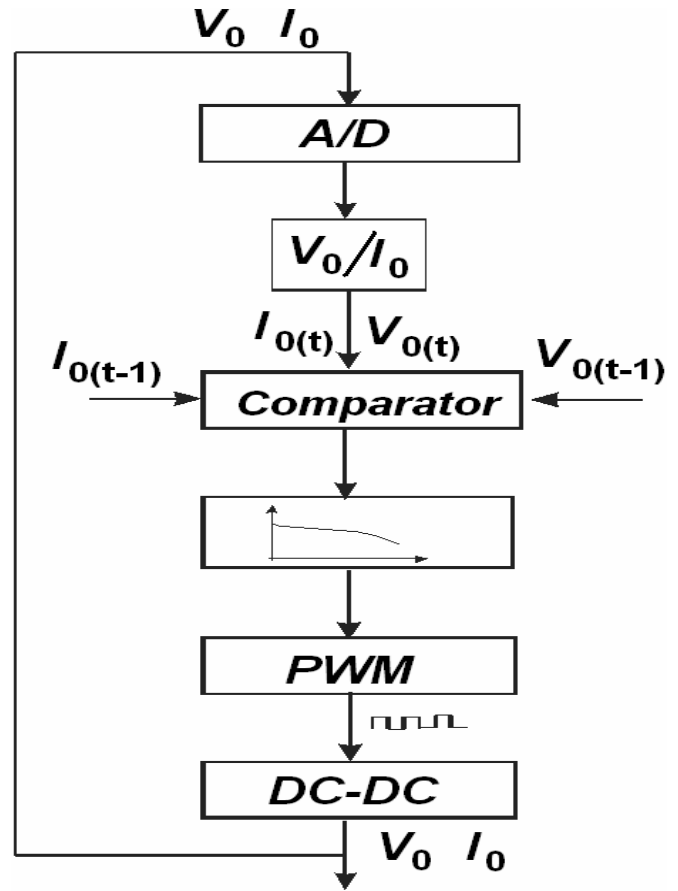

Fig. 7. Block diagram of the control algorithm.

V. SIMULATION RESULTS

The extensive simulations of the proposed model have been performed using the PROTEUS PROFESSIONAL. Some of the results are shown below.

The schematic used to obtain the dynamic characteristics is shown in Fig. 8.

First, we have increased the ideal stack voltage to 12 V, and

the active cell area by 5 (to support the current of 5 A). These values are multiples of the initial polarization characteristics implemented in the PIC memory. The microcontroller PIC16F877 measures current I_0 and voltage V_0 and with the software, implemented in its memory, creates PWM pulses for driving the buck converter. The period of the PWM pulses is constant and was chosen to be 25 kHz. The pulse width is controlled by the implemented polarization curve and measured values of the output current, I_0, and voltage, V_0. The output voltage varies from 12 V, at system idle, to about 5V, at rated current of 5 A. The simulation results of the static $V–I$ characteristics are shown in Fig. 9.
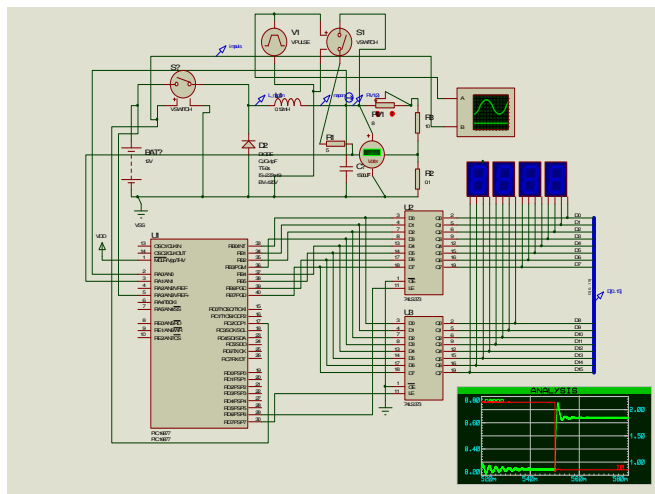
Fig. 8. The schematics presentation of the simulated circuit in PROTEUS PROFESSIONAL.
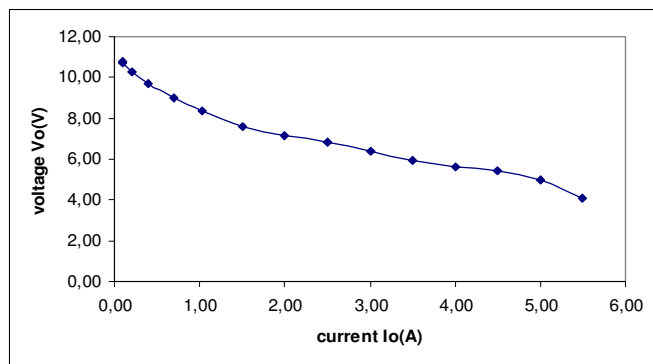
Fig. 9. Simulated V-I characteristic for PEM fuel cell model (12V/5A).

The dynamic response of the model is very fast and follows the polarized $V–I$ curve of a PEM fuel cell. The step change of the load resistance, from 50 to 2 Ω, resulted in increasing the current to 2.2 A, and the decreasing the output voltage to 6.6 V. The simulation results are shown in Fig. 10.

To examine the operation of our model the simulation results are compared with measured ones, of a commercially available fuel cell system.
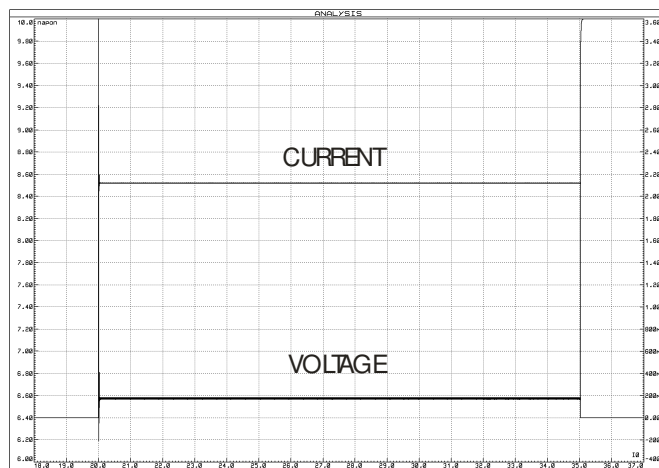
Fig. 10. Simulated waveforms for a dynamic behavior of a PEM fuel cell model.

(a)

(b)
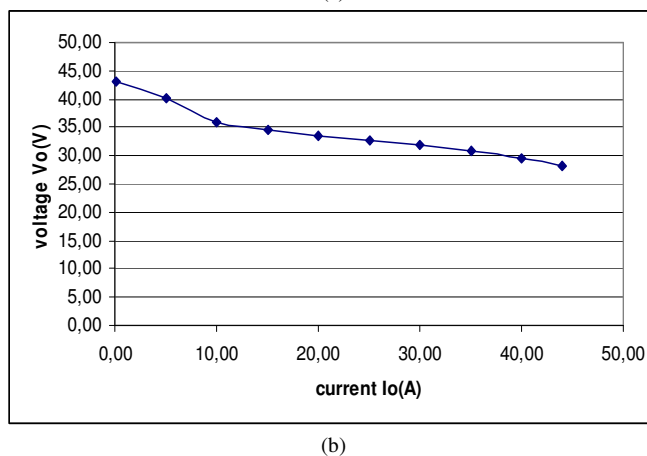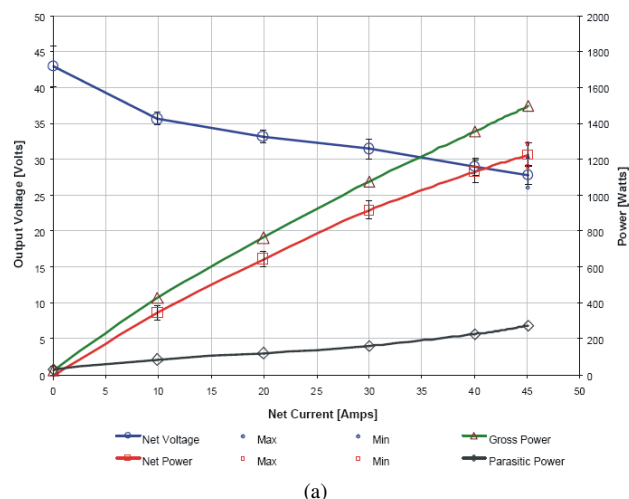
Fig. 11. (a) V-I characteristics of a PEM fuel system obtained from experiment [21], (b) Simulated V-I characteristics of DC-DC converter for maximum voltage 48V and maximum current 45A.

In Fig. 11-(a) we show the polarization characteristics of the Nexa™ system [21]. The output power ranges from zero at system idle to 1200 watts at rated power. The output current varies from zero to 46 A. The output voltage changes with operating load according to the polarization characteristics of the fuel cell stack. Normal idle DC

voltage of the Nexa™ system is approximately 43 V. At rated power, the Nexa™ system DC output voltage ranges from 26 to 29 V.

In Fig. 11-(b) we show the simulated $V{-}I$ characteristics of the DC−DC, buck converter based, PEM fuel cell model adapted to the Nexa™ system. It can be seen that the characteristics corresponds very well to the measured one given in Fig. 11-(a).

VI. Conclusion

A preliminary design of a PEM fuel cell model, based on DC-DC buck converter, suitable for hardware realization has been presented. Due to the digital nature of the control system, it is possible to make quick changes to the mathematical model, thus avoiding changes in the system hardware in most cases. The hardware changes affect only the power stage, when larger stack current and/or voltage have to be obtained. The temperature and pressure characteristics can be easily implemented in this model.

The proposed model can be used in the design process of fuel cell power systems, during simulation or practical realization stages. When realized in practice, this PEM fuel cell simulator can be also used to test power systems designed to interact with PEM fuel cells, in order to prevent stack degradation caused by the electric behavior of the system. Foreseen benefits of this model are the ability to work without reagents in a non-specialized environment, in a reproducible way and with a faster start-up/turn-off operation.

The proposed model has been tested by simulation using the PROTEUS PROFESSIONAL. The model is validated by comparing the simulation and experimental results obtained on a commercial PEM fuel cell module.

By realizing the hardware and further development of the software, using the equations (8) − (16), this model can be transformed into real fuel cell emulator.

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

References

[1] Sharon Thomas, Marcia Zalbowitz, "Fuel Cells – Green Power," *Los Alamos National Laboratory, New Mexico*, 1999.

[2] "Fuell Cells Fact Sheet," *Enviromental and Energy Study Institute, Washington DC*, February 2000.

[3] Y. R. Novaes, I. Barbi, "Low Frequency Ripple Current Elimination in Fuel Cell Systems", *2003 Fuel Cell Seminar Proceedings,*" Miami, November, 2003, pp. 21-26.

[4] S. Yerramalla, A. Davari, A. Feliachi, "Dynamic modeling and analysis of polymer electrolyte fuel cell", *Proc. IEEE Power Engineering Soc. Summer Meeting*, vol. 1, 2002, pp. 82–86.

[5] J.B. van der Merwe, C. Turpin, T. Meynard, B. Lafage, "The installation, modeling and utilization of a 200W PEM fuel cell source for converter based applications", *Proc. IEEE Power Electronics Specialists Conference, 2002*, pp. 333–338.

[6] K. Dannenberg, P. Ekdunge, G. Lindbergh, "Mathematical model of the PEMFC", *J. Appl. Electrochem.* 30 (2000) pp. 1377–1387.

[7] A. Kazim, H.T. Liu, P. Forges, "Modeling of performance of PEM fuel cells with conventional and interdigitated flow fields", *J. Appl. Electrochem.* 29 (1999) pp. 1409–1416.

[8] W. Turner, M. Parten, D. Vines, J. Jones, T. Maxwell, "Modeling a PEM fuel cell for use in a hybrid electric vehicle", *Proc. IEEE Vehicular Technology Conference*, 1999, pp. 16–20.

[9] R. Gemmen, P. Famouri, "PEM fuel cell electric circuit model", *Proc. of the Power Electronics for Fuel Cells Workshop*, 2002.

[10] D. Yu, S. Yuvarajan, "Electronic circuit model for proton exchange membrane fuel cells", *Journal of Power Sources* 142 (2005). pp. 238–242.

[11] A. Capel, J. Calvente, R.Giral1, H. Valderrama-Blavi, A. Romero, and L. Martínez-Salamero, "Modeling of a Fuel Cell as an Energy Source Power System*" Proc SAAEI* 2006, pp. 64-68.

[12] G. L. Arsov, "Parametric Pspice Model of a PEM Fuel Cell" *Electronics,* Vol. 11 No. 1-2*,* FEE - Banja Luka, Dec 2007, pp. 99-103.

[13] National Energy Technology Laboratory, "*Fuel Cell Hand Book*", sixth ed., 2002, pp. 2.1–2.20.

[14] Sharon Thomas, Marcia Zalbowitz, "Fuel Cells – Green Power," *Los Alamos National Laboratory, New Mexico*, 1999.

[15] "Fuel Cells Fact Sheet," *Environmental and Energy Study Institute, Washington DC*, February 2000.

[16] Andrew R. Balkin, "Modeling a 500 W Electrolyte Membrane Fuel Cell," *University of Technology, Sydney*, June 2002.

[17] J. Larminie, A. Dicks "*Fuel Cell Systems Explained*", Wiley, 2003.

[18] Jay T. Pukrushpan, Anna G.. Stefanopouplu, Huei Peng "*Control of Fuel Cell Power Systems*", Springer, 2005.

[19] Microchip, *PIC16F87X Data Sheet*.

[20] Abraham I. Pressman "*Switching Power Supply Design*", McGraw-Hill, 1998.

[21] *Ballard Power System "NexaTM Power Module Integration Guide", 2002.*

Application of Impedance Spectroscopy for Electrical Characterization of Ceramics Materials

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Abstract—The choice of the most suitable equivalent electrical circuit to model the impedance response of lanthanum doped BaTiO₃ ceramics was emphasized in this paper. The method for the determination of the starting values for the basic equivalent circuit was also presented. These starting values were used in the fitting procedure of experimental impedance data with simulated data in order to select the most correct and appropriate equivalent circuit.

Index Terms—BaTiO₃ ceramics, Impedance spectroscopy, Equivalent circuit.

I. INTRODUCTION

IMPEDANCE spectroscopy (IS) offers an effective method for the characterization of electrical properties of electroceramics especially of ferroelectric materials such as BaTiO₃ based ceramics [1-4]. Having in mind that these materials are used in polycrystalline form, which is characterized primarily by the grain boundaries and grains (bulk), it is necessary to undesrtand the role and the effects of different microstructural features on the overall electrical properties of materials [3-5]. The resistance and capacitance values of bulk and grain boundary, which are frequency and temperature dependent, can be evaluated from IS spectra. Experimental data can be analysed through four possible complex formalisms that represent the same information yet expressed in various ways. Data can be represented through electrical impedance Z^*, electric modulus M^*, admittance Y^*, and dielectric permittivity ε^*. The relationship between them is given as

$$M^* = j\omega C_0 Z^* = j\omega C_0 \left(1/Y^*\right) = 1/\varepsilon^* \qquad (1)$$

where: $\omega = 2\pi f$ is angular frequency, $C_0 = \varepsilon_0 S/d$ vacuum capacitance of the cell without sample, ε_0 is the permittivity of free space, 8.85×10^{-12} F/m, and S and d are area and thickness of the sample, respectively.

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To extract the informations about the resistive and capacitive values of grain and grain boundary regions it is necessary to adopt such electrical model that most precisely represents electrical characteristics of the considered material at different frequencies and at different temperatures. The choice of the adequate model subsumes that the acquired simulation results have to be consistent with experimental data, and is largely based on designer's experience. The acquired values of the model elements have to be real, logical and expected.

The main objective of this study is the strategy of choosing the correct model for the interpretation of IS data. The comparison between models, represented through equivalent electrical circuits, regarding their precision and possibilities of models for optimal fitting of experimental data, is also emphaised. For impedance spectroscopy measurements BaTiO₃ doped with lanthanum (La-BT) was used as an example. La-doped BaTiO₃ was sintered at1300ºC for 2 hours. Impedance measurements were made after the samples had been placed in a furnace at selected temperature for 30 min. IS measurements were perfomed at room temperature, 200, 300 and 350ºC in a frequency range from 20 Hz to 1.0 MHz using LCR-meter Agilent 4284A [6].

The multidimensional Simplex identification algorithm and in-house made software were used for fitting and simulation process of IS data [6,7].

II. BASIC EQUIVALENT CIRCUIT TO MODEL IS DATA OF LA-BATIO₃ CERAMICS

In modeling of IS response for doped and undoped ceramic it is possible to chose more than one equivalent circuit that contains at least the bulk and grain boundary elements [1,3,4]. Therefore, at the very beginning of the analysis the solution is not straightforward. Numerically it is possible for simulated curves to coincide with experimental data by applying different models. However, only one of those solutions represents a real model of electrical behavior of ceramic materials. Concerning BaTiO₃ ceramics, the total ceramic impedance is mainly influenced by grain impedance and grain boundary impedance. Hence, it is assumed that impedance data can be presented with the most simple, yet often satisfying basic equivalent circuit consisting of two parallel resistor-

capacitor (*RC*) elements connected in series, as shown in Fig.1, [1,3]. One of these impedances relates to the grain-boundary (R_1,C_1) and the other to the grain (bulk) (R_2,C_2).
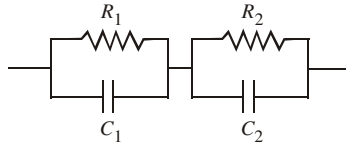

Fig. 1. Basic equivalent circuit to model IS of La-BT ceramics

In the case where the contact resistance of the sample-electrode interface can not be ignored, it is necessary to take into consideration another (*RC)* element connected in series with two other mentioned elements. Since the contribution of sample-electrode interface impendance to the overall IS response is usually very small, in this analysis it is not taken into account.

Complex impedance for circuit given in Fig.1 is:

$$Z^* = Z' - jZ'' = \frac{1}{1/R_1 + j\omega C_1} + \frac{1}{1/R_2 + j\omega C_2} \qquad (2)$$

where:

$$Z' = \frac{R_1}{1 + (\omega R_1 C_1)^2} + \frac{R_2}{1 + (\omega R_2 C_2)^2} \qquad (3)$$

$$Z'' = R_1 \frac{\omega R_1 C_1}{1 + (\omega R_1 C_1)^2} + R_2 \frac{\omega R_2 C_2}{1 + (\omega R_2 C_2)^2} \qquad (4)$$

On the basis of expression $M^* = j\omega C_0 Z^* = M' + jM''$ the components of electrical moduls are easily obtained:

$$M' = \frac{C_0}{C_1} \frac{(\omega R_1 C_1)^2}{1 + (\omega R_1 C_1)^2} + \frac{C_0}{C_2} \frac{(\omega R_2 C_2)^2}{1 + (\omega R_2 C_2)^2} \qquad (5)$$

$$M'' = \frac{C_0}{C_1} \frac{\omega R_1 C_1}{1 + (\omega R_1 C_1)^2} + \frac{C_0}{C_2} \frac{\omega R_2 C_2}{1 + (\omega R_2 C_2)^2} \qquad (6)$$

In order to estimate the *RC* values for each element it is necessary to observed concurrently the impedance Z^* and electrical modulus M^* of the samples. This is because each parallel *RC* element contributes to the shape of impedance spectra in a different way, most often in the shape of semicircular arcs in $Z''(Z')$ and $M''(M')$ complex plane or in the shape of peaks in spectroscopic plots of the imaginary components $Z''(\log f)$ and $M''(\log f)$ which will be discussed later. In addition, to get a straightforward model, valuated both at different frequencies and different temperatures, the influence of individual *R* and *C* parameters onto the impedance and electrical modulus of the discussed ceramics, have to be considered. The influence of *RC* parameters on the impendance shape is illustrated in Figs. 2 and 3.

Fig. 2 shows the imaginary and real parts of impedance $Z''(Z')$ in complex plane for the case where the same capacitance values ($C_1 = C_2$) are chosen, while the value of resistance R_2 remains constant and resistance R_1 changes. The analysed characteristic at such conditions contains only one set of semicircles whose shape and dimensions are determined by dominant resistance (in this case R_1). In the case of different *C* values, $C_1 < C_2$ of semicircles lines appear on impedance complex plane, as shown in Fig. 3. The shape of curves is

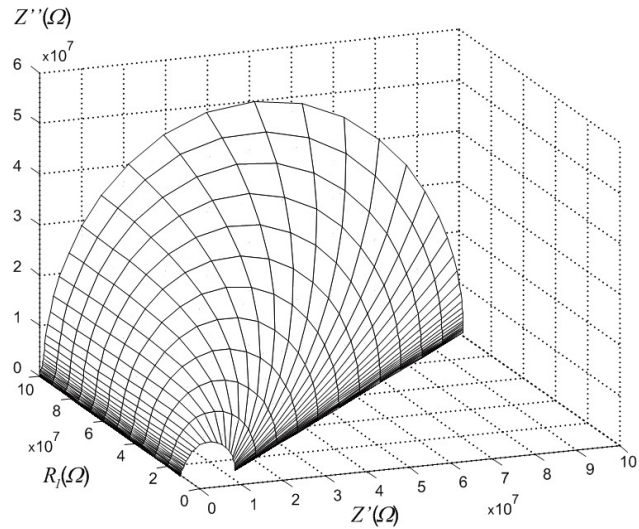determined by the dominant value of resistance, here that is also resistance R_1.

Fig. 2. Impedance of equivalent circuit from Fig.1 shown in complex plane $Z''(Z')$, where: $C_1 = C_2 = 10^{-12}$F, $R_2 = 10^6 \Omega$, and R_1 changes in the range from $5 \times 10^6 \Omega$ to $10^8 \Omega$

By the analysis of electrical modulus of impedance $M''(M')$, in function of relative relation of equivalent circuit elements, the similar results were obtained, as given in Figs. 4 and 5.

Fig. 4 presents the analysis of electrical impedance modulus in the case of equal resistance values $R_1 = R_2$, while capacitance value C_2 changes at fixed capacitance value C_1. In this case only one set of semicircle lines is obtained whose shape and size are primarily determined with that *RC* element which has lower capacitance value (now that is C_2 capacitance). In other words, if one capacitance is much higher than another, semicircle arc attached to it in complex plane $M''(M')$ is lost. Fig. 5 shows an example of electrical modulus in the case of mutually different fixed resistance values R_1 and R_2, at the change of C_2 capacitance (C_1 is also fixed). In this case the considered charachteristic contains two sets of semicircle arcs. Here too, the dominant effect onto the shape and appereance of secondary arc has the *RC* element with smaller capacitance value (that is C_2).
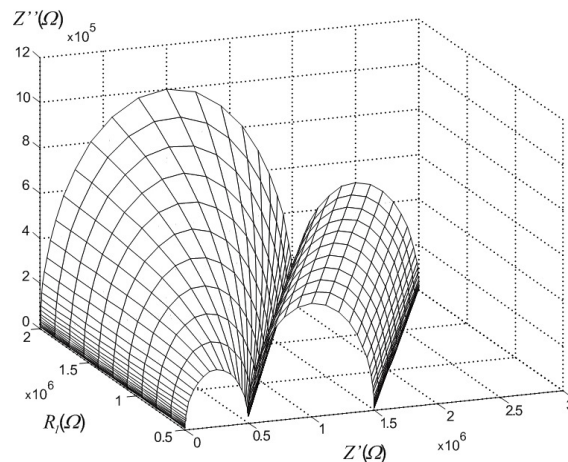

Fig. 3. Impedance of equivalent circuit from Fig.1 shown in complex plane $Z''(Z')$, where: $C_1 = 10^{-12}$F, $C_2 = 10^{-9}$F, $R_2 = 10^6 \Omega$, and R_1 changes in the range from $0.5 \times 10^6 \Omega$ do $2 \times 10^6 \Omega$
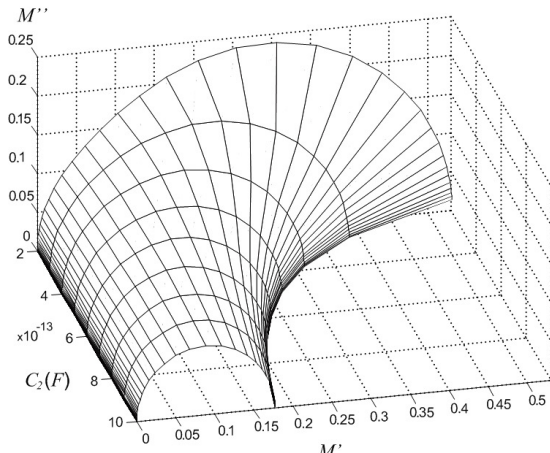
Fig. 4. Electrical modulus of equivalent circuit from figure 1 shown in complex plane M''(M'), where: $R_1= R_2=10^6\Omega$, $C_1=10^{-12}$F, and C_2 changes in the range from 0.2×10^{-12}F to 10^{-12}F
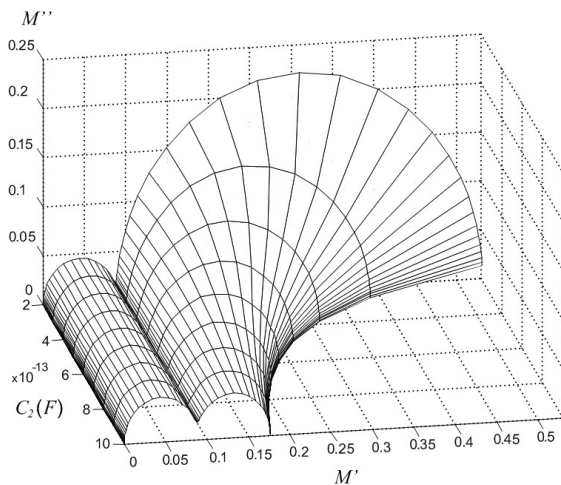

Fig. 5. Electrical modulus of equivalent circuit from figure 1 shown in complex plane M''(M'), where: $R_1=10^8\Omega$, $R_2=10^6\Omega$, $C_1=10^{-12}$F, and C_2 changes over the range 0.2×10^{-12}F to 10^{-12}F

The previous analysis demonstrates the usefulness of concurrent visual inspection of spectroscopic plots of $Z''(Z')$ and $M''(M')$. It has to be said that this comparison is not always simple, because with the increase of frequency the dots on curves in $Z''(Z')$ complex plane, move towards coordinate center (Figs. 2,3), while with the increase of frequency, the dots on curves in $M''(M')$ complex plane, move away from coordinate center (Figs. 4,5).

III. DETERMINING THE VALUES OF THE BASIC EQUIVALENT CIRCUIT ELEMENTS

During determining of equivalent circuit elements, based on experimental impedance spectra, various cases can occur. It should be noted that most often only modulus and the angle of their impedance are measured for ceramic materials. On the basis of these measurements, it is very demanding to distinguish values of certain elements of equivalent circuit. Which of RC elements, of the basic equivalent circuit from Fig. 1, will be detected depends on the characteristic being considered, as well as on relative relation of the equivalent

circuit elements values, as analysed already in Figs. 2-5. While impedance characteristic is more appropriate for determining RC element with higher resistance, electric modulus is more appropriate for determining RC element with lower capacitance.

Here follows an example of determining the model's parameters for basic equivalent circuit, using experimental IS data obtained for La-doped $BaTiO_3$ ceramics. Because of the limited frequency range of equipment, the IS spectra obtained at lower temperature are incomplete, whereas spectra obtained at higher temperatures showed satisfactory quality. Measurments perfomed at 350^oC over the frequency range from 20 Hz to 1.0 MHz are used in further analysis.

Three-dimensional (3D) image of IS spectrum, obtained at 350^oC, together with two-dimensional (2D) projections of imaginary $Z''(\log f)$ and real parts $Z'(\log f)$) of impedance in a function of frequency, and also 2D $Z''(Z')$ impedance in a complex plane, are given in Fig. 6.
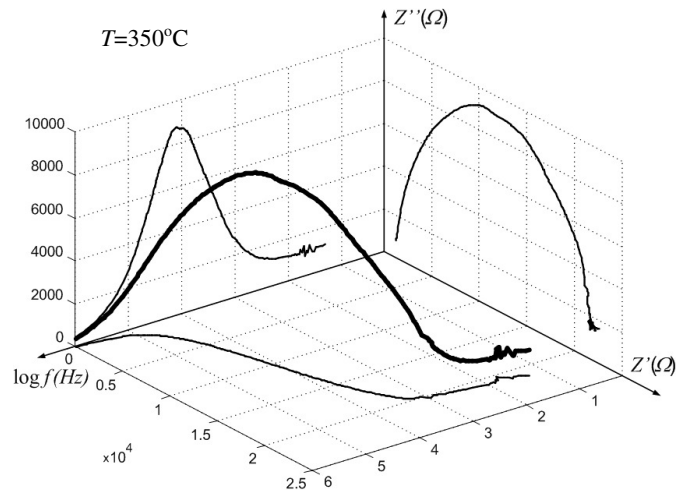
Fig. 6. 3D image of experimental impedance characteristic of the measured sample and 2D images of its projections

For the sake of clarity, measured impedance spectrum $Z''(Z')$ in a complex plane, for the same La-BT sample, is again presented in Fig. 7 (the curve is denoted with open circles). On the basis of visual inspection of IS spectrum shown in Fig.7 with those shown in Figs. 2 and 3, it can obviously be concluded that this is the case when $R_1 \gg R_2$, as the measured IS spectrum contains only one semicircle arc. Applying the basic equivalent circuit, given in Fig. 1, the simulated spectrum is obtained and presented with curve (a) in Fig. 7. The total resistance of the circuit can easily be read from the curve, and it is $R_u=R_1+R_2 \approx R_1=21$ kΩ. The presented spectrum allows for the determination of only total resistance of sample R_u.

Determination of other circuit parameters includes a consideration of the imaginary components of impedance and electric modulus $Z''(\log f)$ and $M''(\log f)$ as a function of frequency (Fig. 8). By direct comparison of spectroscopic plots, obtained on 350^oC, it can be seen that electric modulus $M''(\log f)$ has two peaks over the investigated frequency range, and that lower frequency $M''(\log f)$ peak coincides to that of $Z'(\log f)$ peak. The peaks in the $Z'(\log f)$ and $M''(\log f)$ plots are known as Debye peaks. It can also be noted that the advantage

of the combined analysis of both dependences is in the fact that the peaks of these characteristics, that correspond to each of RC elements, can overlap on frequency scale, as is the case here with $M''(\log f)$ and $Z''(\log f)$ peaks (Fig.8). In this particular case both RC elements determine the electric modulus peaks, while the impedance peak is determined by the element with higher resistance. The frequency at the Debye peak maxima for each RC element is given by the expression $2\pi f_{\max} RC = 1$.
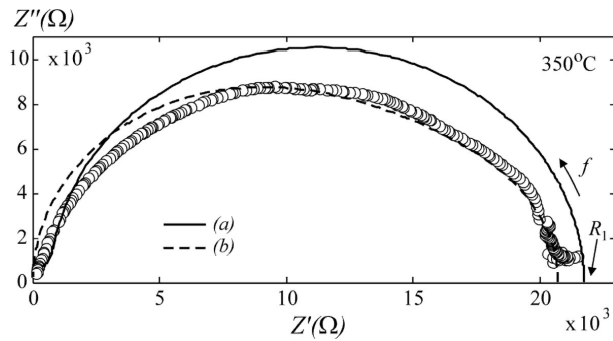
$$Z''(\Omega)$$

Fig. 7. Experimental AC impedance spectrum in complex plane (presented with open circles) for La-BT at 350°C, modelled impedance spectrum using the calculated values of circuit elements (a) and for fitted values (b)

Capacitance values in equivalent circuit can more precisely be determined by using the spectroscopic plot of electric modulus in a complex plane, shown in Fig. 9. That spectrum presents the connection between two incomplete semicircles arcs and corresponds to the case given in Fig. 5, where $R_1 \gg R_2$, and C_2 is somewhat higher than C_1. Therefore, in this way, according to graphs from Figs. 7 and 8, and their comparison with Figs. 2 to 5, relative ratios of equivalent circuit elements are determined. That is, it is assumed that the equivalent circuit from figure 1 is satisfactory for application in this case too.

Capacitance values can be estimated from the intercept of idealized M'' curve (presented by broken line in Fig. 9) with M' axis: In the concrete case, according to Fig. 8, $M''(\log f)$ maximum correspond to $\log f_{1max}=4.16$, and:

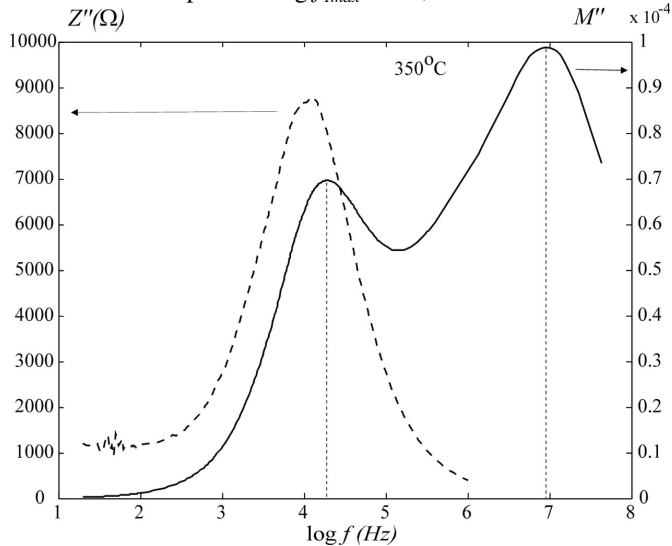$$Z''(\Omega) \qquad\qquad\qquad M'' \quad \text{x}10^{-4}$$

Fig. 8. Impedance Z'' and electric modulus M'' of the measured sample in funcion of frequency

$$C_1 = \frac{1}{2\pi f_{1\max} R_1} = 524.33 \ \text{pF} \qquad (7)$$

$$C_1 = 8.85 \cdot 10^{-14} / 1.7 \cdot 10^{-4} = 520.59 \ \text{pF} \qquad (8)$$

which is close to the value calculated by equation 7. From Fig. 9, it also follows that:

$$8.85 \cdot 10^{-14}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) = 5.7 \cdot 10^{-4} \qquad (9)$$

so the capacitance C_2=220.58 pF.
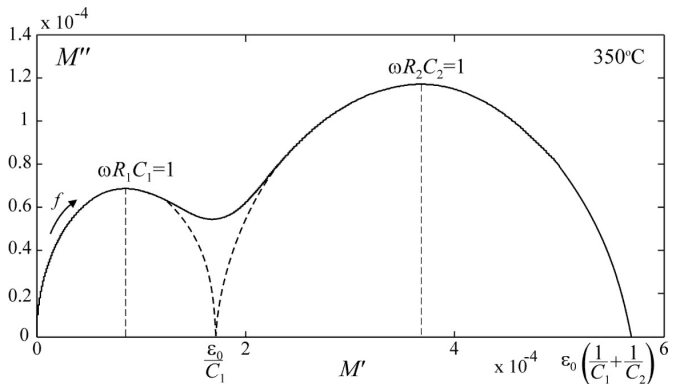
Fig. 9. Experimental characteristic of impedance Z'' and electric modulus M'' of the measured sample as a function of frequency

To determine the resistance (R_2) there is a need again for the combined analysis of dependence $M''(\log f)$ from Fig. 8 and $M''(M')$ from Fig. 9. The resistance R_1, already calculated from Fig. 7, is approximately equal to R_u=21Ω. The R_2 value can be calculated using expression $2\pi f_{2\max} R_2 C_2 = 1$. As from Fig. 8: $\log f_{2max}$=6.9, and C_2=220.58 pF, the required resistance value for R_2 is R_2=90.83Ω.

The presented algorithm of calculating the basic circuit elements can be used for IS spectra obtained at any temperature. The frequency dependence of M'' values for La-BaTiO$_3$ ceramic sample at selected temperatures is given in Fig. 10.

At lower temperatures only one peak can be noted on a M'' plots, however, at higher temperatures this peak has a tendency to split into two peaks whose positions move towards higher frequences with temperature increase. The lower frequency peak has approximately the same amplitude which indicates that capacitance that determines it does not change with the increase of temperature, while higher frequency peak rises with temperature increase, which means that capacitance that determines it decreases with the increase of temperature. These results show that at higher temperatures both parallel RC elements significantly contribute to equivalent circuit impedance, as then differences between RC elements are greater. At lower temperatures the differences between RC elements are smaller, and only one frequency peak characterizes Z' and M' plots, as noted earlier in Figs. 2 to 5.

Fig. 10. Electric modulus M" of sample as a function of frequency for selected temperatures

By applying the previously described procedure, the approximate values of equivalent circuit elements can be gained for any of selected temperature. In accordance with previously presented analysis, it can be assumed that the equivalent circuit from 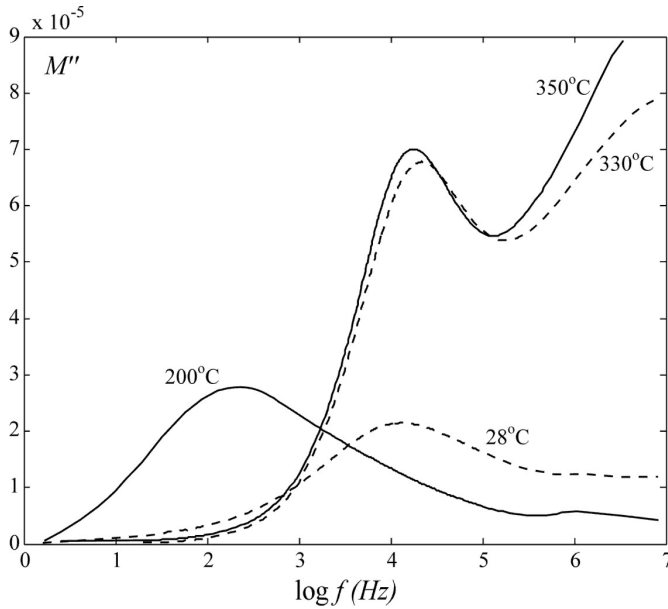Fig. 1 is highly real. It can also be assumed that elements R_1C_1 and R_2C_2 represent two different part in microstructure of ceramics. It is very well known that grain boundary resistance is higher compare to grain/bulk, so it is for believe that R_1C_1 and R_2C_2 elements of basic equivalent circuit, (Fig.1), correspond to grain boundary and grain region respectively. To illustrate the extent of accuracy of this way of modelling, the simulated spectrum $Z''(Z')$, using already calculated parameters R and C, is shown as a curve (a) in Fig. 7. It is obvious that there is a significant deviation of modelled and experimental IS spectrum, because with the previous procedure only approximate values of equivalent circuit elements could be obtained.

One of the method to increase the accuracy and precision in determination of RC values is to use a method of models parameters identification by means of fitting experimental and theoretical data using multidimensional identification algorithm, such as multidimensional Simplex method [6,7]. The $Z''(Z')$ plot, presented as a curve (b) in Fig. 7, was obtained by applying this fitting method, and the corresponding R and C values were as follows: $R_1 = 14.80$ kΩ, $C_1 = 714.63$ pF, $R_2 = 5.93$ kΩ, $C_2 = 7.98$ nF.

The discrepeance between experimental and simulated IS spectra (Fig.7) leads to the conclusion that the basic equivalent circuit needs adjusting, or that there needs to be applied a more complex model than the usual one given in Fig. 1. On the other hand, it can be concluded that impedance $Z''(Z')$ in reality does not have the shape of ideal semicircle arc. Due to that, here follows the consideration on the possibility of applying different equivalent circuit models capable for better simulation of impedance spectra of doped $BaTiO_3$ ceramics.

IV. ANALYSIS OF MORE COMPLEX CIRCUIT MODELS

Impedance response of ceramic materials could be rarely presented by an ideal semicircle arc and treated of simple parallel RC elements. As already indicated, for doped $BaTiO_3$ taken as an example, the arc in complex impedance Z'' vs. Z' dependence is not ideal (Fig. 7). For a low frequency range a semicircle arc is depressed with its centre below the real axis. To model the IS spectra that contain the semicircle arc and distorted part of this arc, a modified equivalent circuit is proposed and corresponding simulated impedance spectra are given in Fig. 11. It has to be noted that a basic equivalent circuit, that can be presented with two parallel RC elements serially connected refers to the ideal "Debye" like ceramic behavior. In the real case the ceramic materials do not manifest the ideal "Debye" like behavior, thus to illustrate more fully the deviation from an ideal capacitor, an additional element with constant phase (CPE) is introduced into equivalent circuit [3,4]. CPE element is used to explain phenomena on the grain boundary areas on one side, and phenomena relating to unhomogeneity, diffusion processes or stress that occurs in the sample, on the other side. For the non ideal "Debye" like behavior in ceramic materials, CPE-element is introduced mainly instead of ideal capacitor or as an addition to the parallel RC connection. Impedance of CPE-elements can be determined as:

$$Z^*_{CPE} = [A(j\omega)^n]^{-1} \qquad (10)$$

Where A is a constant that is independent of frequency, and n is an exponential index that is the measure of distortion of $Z''(Z')$ characteristics. For an ideal "Debye" like behavior, it stands that $n=1$, and CPE represents an ideal capacitor with the value $C=A$. The value of n bellow 1 indicates that the capacitor is frequency dependent. For $n=0$, CPE behaves like pure restistance with the value $R=1/A$.

The relation between parameters of equivalent circuit (R, n, A) and curve parameters (x, y, ω_{max}) are shown in Fig. 11.
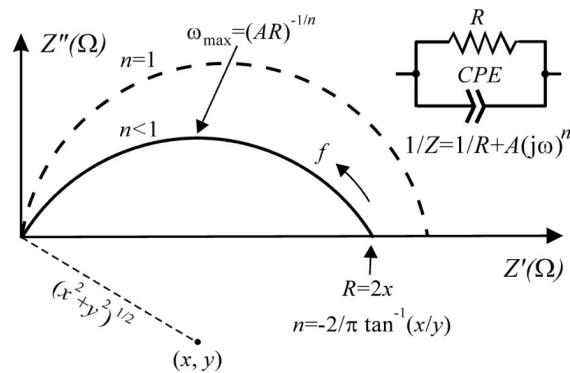
Fig. 11. Modelled complex impedance characteristic for equivalent R-CPE circuit, shown as inset in the image

The calculated values of all impedance formalisms of an equivalent circuit, given in expression (1) have to be identical with the values of impedance formalisms as measured on the sample. Several different equivalent circuits can be suggested for the same sample and the choise of the satisfactory equivalent circuit has to be realised on the basis of additional information.

Besides the basic circuit, with two parallel *RC* elements, the five more equivalent circuits with *CPE* elements have been chosen for the purpose of modelling impedance characteristics for La-BT ceramics. The proposed electrical circuits together with the expression for total impedance *Z** are given in Fig. 12. Multidimensional Simplex identification algorithm, realized with Matlab tools, [6,7] was used for fitting procedure and determination of model's parameters.

(a)

$$Z^* = 1/(1/R_1 + j\omega C_1) + \\ + 1/(1/R_2 + j\omega C_2)$$

R_1=14.80kΩ, R_2=5.93kΩ, C_1=714.63pF, C_2=7.98nF

(b)

$$Z^* = 1/\left(1/R_1 + A_1(j\omega)^{n1}\right) + \\ + 1/(1/R_2 + j\omega C_2)$$

R_1=12.88kΩ, R_2=9.22kΩ, A_1=22.52nF, C_2=1.31nF, n_1=0.75

(c)

$$Z^* = 1/\left(1/R_1 + A_1(j\omega)^{n1}\right) + \\ + 1/\left(1/R_2 + A_2(j\omega)^{n2}\right)$$

R_1=13.55kΩ, R_2=8.57kΩ, A_1=1.63nF, A_2=63.16nF, n_1=0.95, n_2=0.71

(d)

$$Z^* = 1/(1/R_1 + j\omega C_1 + A_1(j\omega)^{n1}) + \\ + 1/(1/R_2 + j\omega C_2)$$

R_1=13.22kΩ, R_2=9.11kΩ, C_1=394.11pF, A_1=56.56nF, C_2=1.41nF, n_1=0.64

(e)

$$Z^* = 1/\left(1/R_1 + j\omega C_1 + A_1(j\omega)^{n1}\right) + \\ + 1/\left(1/R_2 + A_2(j\omega)^{n2}\right)$$

R_1=22.78kΩ, R_2=1.88kΩ, C_1=698.33pF, A_1=894.12nF, A_2=23.68nF, n_1=0.27, n_2=0.79

(f)

$$Z^* = 1/\left(1/R_1 + j\omega C_1 + A_1(j\omega)^{n1}\right) + \\ + 1/\left(1/R_2 + j\omega C_2 + A_2(j\omega)^{n2}\right)$$

R_1=21.32kΩ, R_2=365.14Ω, C_1=424.46pF, C_2=223.16pF, A_1=11.75nF, A_2=219.68nF, n_1=0.67, n_2=0.63
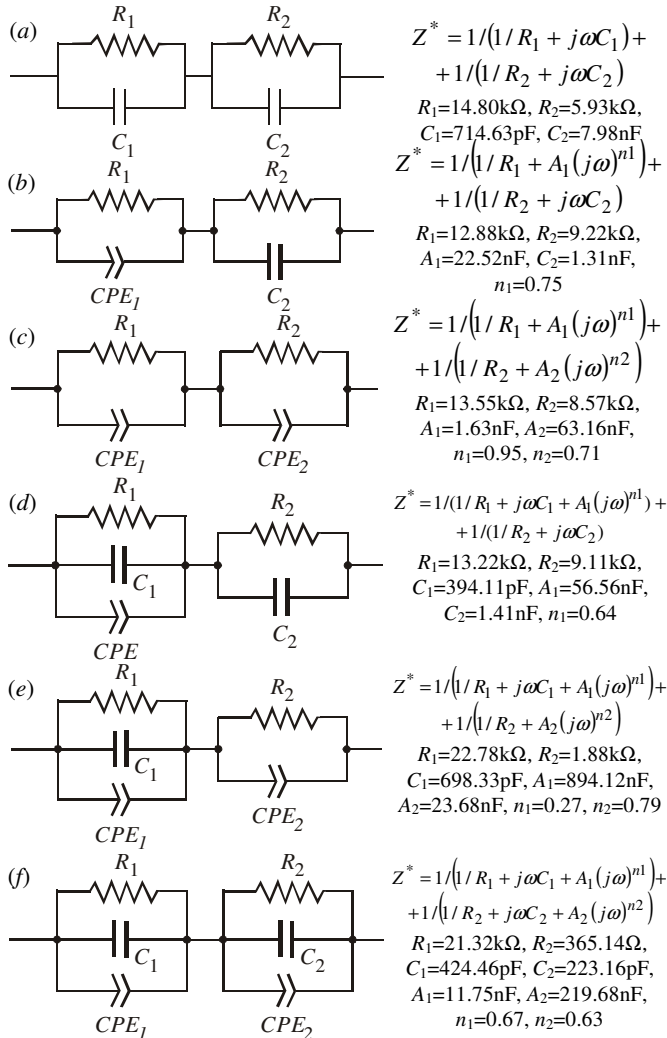
Fig. 12. Various equivalent circuits to model La-BT ceramic

The impedance formalisms for all analysed circuits are shown in Fig. 13. As can be seen from Fig. 13, a fairly good agreement between experimental and modelled results, for all impedance formalisms, is obtained by applying an equivalent circuit with two parallel *R-CPE* elements that are serially connected, i.e., the circiut denoted as circuit (c) in Fig. 12. To determine model's parametes of all circuits given in Fig. 12, the initial values of each *RC* elements or *R-CPE* parallel connection are established according to the procedure from chapter 3. The initial values for *A* and *n*, in circuits 12*b* to 12*f*, are established on the basis of measured data from the real part of admittance *Y* [3]. The obtained initial parameters values, for all applied circuits, have been refined to get the best possible fitting of experimental data.
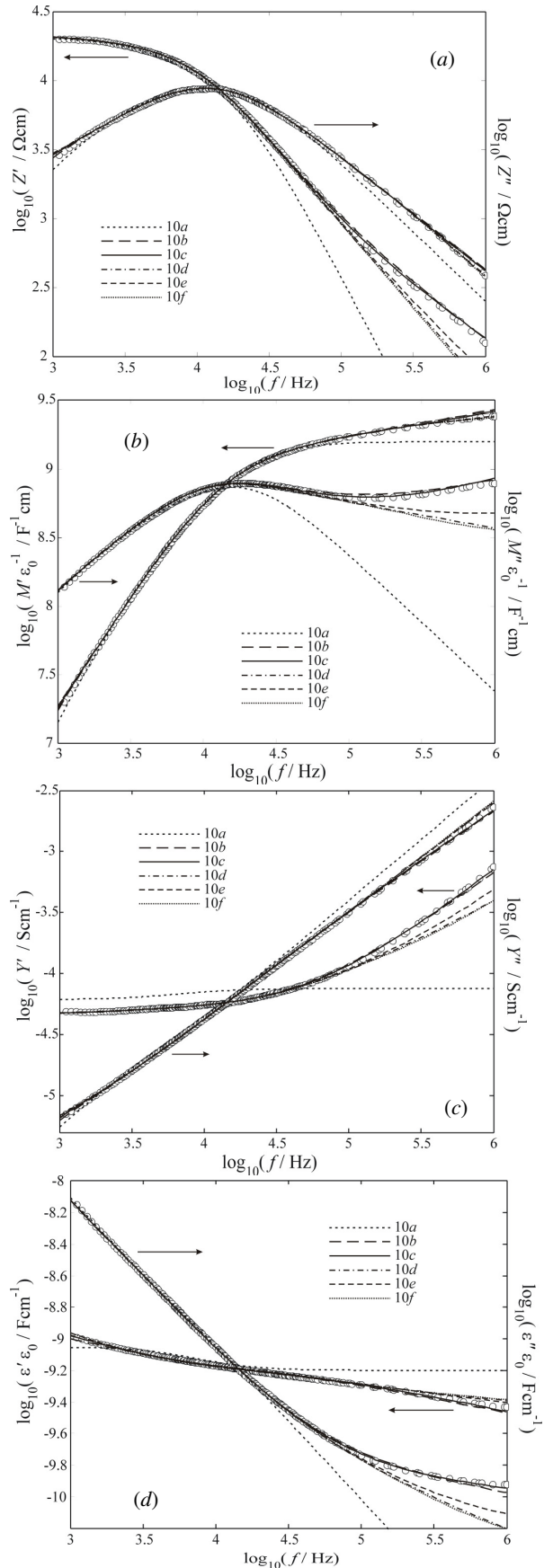

Fig. 13. Normalised frequency dependences of real and imaginary impedance parts for (a) Z*, (b) M*, (c) Y* and (d) ε*, in log-log ratio, measured at 350°C (circles), and modeled results obtained through best fitting for equivalent circuits presented in figure 12 (colored lines)

Typical results obtained through fitting procedure of equivalent circuits parameters are shown with a full line, while experimental data are marked with open circles. The significant deviation, at lower and higher frequencies, between experimental and simulated values, was obtained with equivalent circuits (*a*), (*d*) and (*e*), in comparison with results gained with other circuits, especially as related to the circuit (*c*) given in Fig. 12.

III. CONCLUSION

The impedance responce of La-doped $BaTiO_3$ ceramics were interpreted in terms of basic equivalent circuit with two *RC* elements connected in series and another five proposed equivalent circuits that contain resistors, capacitor and *CPE* elements. By the analysis of equivalent circuit impedance, combined with the analysis of experimental data of electrical modulus, it was possible to extract the resistance and capacitance contribution of grain and grain boundary regions to the overall electrical properties of doped $BaTiO_3$ ceramics. The method of determining initial values of basic eqivalent circuit elements of ceramic materials was presented. For the basic equivalent circle these values presented the initial parameters during the process of fitting the experimental and simulated impedance in order to get a more precise model.

Final adjustment of model parameters was performed by identification of unknown parameters applying multidimensional Simplex algorithm realised in Matlab. Satisfactory agreement between theoretical and experimental results was gained by applying an equivalent circuit that has two parallel *R-CPE* elements serially connected. The circuit paramer n, being lower than one, $0.95 \leq n \geq 0.63$, highlights the capacitive nature of grain and grain boundary. The grain boundary resistance is higher than the same one of grains.

There is also a discussion on the applicaton and justification of application of several more complex models of this ceramic. Better investigation results would be obtained with an analysis in the wider frequency range than the available one in this case.

ACKNOWLEDGMENT

REFERENCES

[1] A.J.Moulson, J.M.Herbert, Electroceramics, New York, Willey Press, 2003.

[2] E.Barsoukov, J.R.Macdonald, Impedance Spectroscopy: Theory, Experiment, and Applications, New York, John Wiley & Sons, 2005.

[3] A.R.West, D.C.Sinclair, N.Hirose, "Characterization of Electrical Materials, Especialy Ferroelectrics, by Impedance Spectroscopy", Journal of Electroceramics, vol. 1:1, pp. 65-71, 1997.

[4] E.J. Abram, D.C. Sinclair and A.R. West, "A Strategy for Analysis and Modeling of Impedance Spectroscopy Data of Electroceramics: Doped Lanthanum Gallate", Journal of Electroceramics, 10, pp.165-177, 2003

[5] N. Hirose, A. R. West, "Impedance Spectroscopy of Undoped $BaTiO_3$ Ceramics", J.Am.Cer.Soc. V. 97 [6], pp. 1633-1641, 1996.

[6] D.Mančić, V.Paunović, M.Vijatović, B.Stojanović, Lj.Živković: "Electrical Characterization and Impedance Response of Lanthanum Doped Barium Titanate Ceramics", Science of Sintering, pp. 283-294, 2008.

[7] D.Mančić, M.Radmanović, V.Paunović, V.Dimić, D.Stefanović: Modeling of PZT Piezoceramic Rings, Science of Sintering, Vol. 30, Spec. Issue, pp. 53-62, 1998.

[8] V. Petrovsky, T. Petrovsky, S. Kamlapurkar, F. Dogan, "Characterization of Dielectric Particles by Impedance Spectroscopy (Part I) ", J.Am.Cer.Soc. V. 91 [6], pp. 1814-11816, 2008.

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Strained Si/SiGe MOS transistor model

Tatjana Pešić-Brđanin, Nebojša Janković

Abstract— **In this paper we describe a new model of surface-channel strained-Si/SiGe MOSFET based on the extension of non-quasi-static (NQS) circuit model previously derived for bulk-Si devices. Basic equations of the NQS model have been modified to account for the new physical parameters of strained-Si and relaxed-SiGe layers. From the comparisons with measurements, it is shown that a modified NQS MOS including steady-state self heating can accurately predict DC characteristics of Strained Silicon MOSFETs.**

Index Terms—**Strained-Si, MOSFET, modeling.**

I. INTRODUCTION

IMPROVEMENT in performance of Si MOSFETs through conventional device scaling has become more difficult, because of several physical limitations associated with the device miniaturization. [1]. Thus, much attention has recently been paid to the mobility enhancement technology through applying strain into CMOS channels [2-4]. Using Hall effect structures, high electron mobility have been measured in strained Si at room temperature and mobility approaching 500 000 cm /Vs has been demonstrated at 0.4 K [5]. Electron mobility enhancements in tensile-strained Si have been theoretically predicted for both bulk and inversion layer transport [6,7].

Strained-Si (SS) technology is emerging as a leading choise for continuous progression of transistor performances. For future circuit applications of these promising devices, the efficient SS MOSFETs modela are required. Consequently, there is a strong interest in the extension of conventional bulk SiMOSFET models to SS devices. A few studies of the extensions of the conventional bulk-Si MOSFET models published so far [8-10] have aimed primarily to estimate the implication of SS devices on final circuits performances. However, the validation of these models with experimental SS device data has not been presented.

In this paper, a new model of SS MOSFET is derived based on our recently described non-quasi-static bulk-Si devices model (the NQS MOS model) [11].

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It aapears that, owning to a small set of parameters directly related with the device underlining physics, the NQS MOS model can be easily modified to include new physical parameters of straines-Si and relaxed-SiGe layers. The modelling results of the modified NQS MOS model will be demonstrated by comparison with the experimental data of both SS NMOSFET and Si-control NMOSFET devices.

II. SS MOSFET

Fig. 1 shows a schematic illustration of the crystal lattice for strained Si on relaxed $Si_{1-x}Ge_x$, and the subsequent energy splitting of the Si conduction band edge. Because the equilibrium lattice constant of $Si_{1-x}Ge_x$ is larger than that of Si, a pseudomorphic layer of Si grown on relaxed $Si_{1-x}Ge_x$ is under biaxial tension. The strain lifts the sixfold degeneracy in the conduction band and lowers the two perpendicular valleys (labeled Δ_2 in Fig. 1) with respect to the four in-plane valleys (Δ_4). Electrons are expected to preferentially occupy the lower-energy Δ_2 valleys, reducing the effective in-plane transport mass. The energy splitting also suppresses intervalley phonon-carrier scattering, increasing the electron low-field mobility.
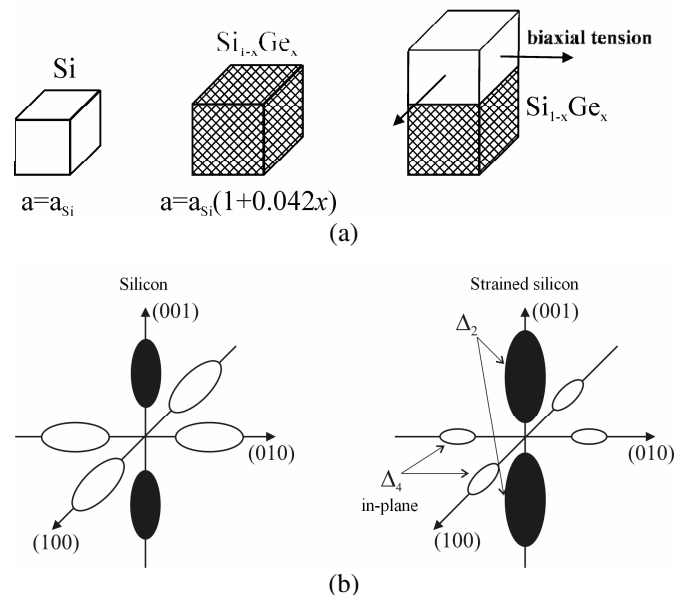

(a)

(b)

Fig. 1. Schematic illustrations of equilibrium lattice, peudomorphic strained Si on relaxed Si1-xGex (b) and strain-induced conduction band splitting in Si.

With the strained-Si layer pseudo-morphycally grown on the relaxed $Si_{1-x}Ge_x$ substrate ('virtual substrate'), the performance

of surface-channel MOSFETs can be greatly enhanced. The main benefit stems from the two effects, the improved carrier mobility and an increased electron saturation velocity. Besides the enhanced mobility, the other important physical parameters of SS and relaxed-SiGe layers (the energy band gap, the band offsets, the dielectric constants etc.) influence the SS MOSFET operation. Thus, compared to its bulk-Si counterpart, the SS NMOSFET exhibits a reduced threshold voltage and significantly higher self-heating effects (SHEs) [13-15].

A schematic cross-section of an experimental surface-channel SS NMOSFET fabricated on relaxed SiGe is shown in Fig. 2 together with its identical bulk-Si counterpart processed simultaneously on Si substrates. These test devices are used for parameters extraction and model validation.
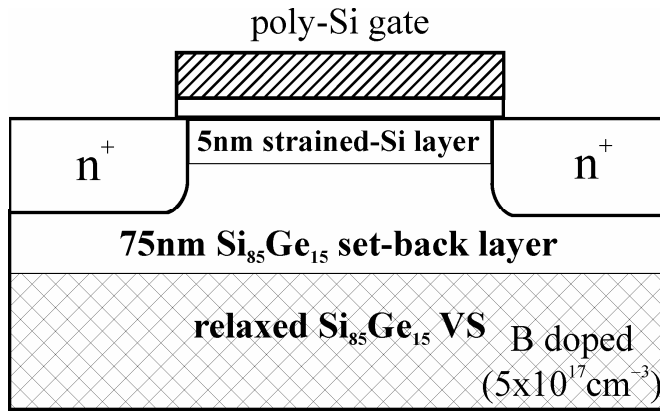

Fig. 2. Schematic cross-section of an experimental surface-channel SS MOSFET fabricated on relaxed $Si_{85}Ge_{15}$ virtual substrate.

Strained-Si n-channel MOSFETs were fabricated on relaxed SiGe virtual substrates with x=15%. The virtual substrates were grown by ultra low pressure CVD in a modified MBE system. A 16–nm strained-Si layer was grown on each virtual substrate, which resulted in a final strained-Si channel thickness of approximately 5 nm due to surface cleans and gate oxidation, as determined by transmission electron microscopy on fully processed devices.

Strained-Si–SiGe device fabrication followed a 0.25μm CMOS process. Active areas were defined in 400-nm deposited oxide, and a gate oxide was thermally grown at 800°C, resulting in a 6 nm gate oxide. Annealing in nitrogen at 800°C was subsequently carried out in order to reduce the gate oxide interface trap density. Polysilicon was deposited and devices down to 150 nm gate length were patterned using electron-beam lithography. As and P were implanted into the source, drain and gate through a thermally grown oxide and annealed at 1050°C for 20 s. Back-end processing comprised deposited silox and BPSG with Al metallization [14].

The modelling of strained-Si devices requires modification of the mobility model, energy band-gap model, as well as relative dielectric constant. Also, due to a poor thermal conductivity (at least fifteen times lower than that of Si of the thick SiGe underlayer) the self-heating effects have to be accounted in the modified NQS model.

III. MODELING THE SS NMOSFETs

In order to extend the NQS MOS model [11] of bulk-Si devices on SS NMOSFETs, some of its basic formulas have to be upgraded to account for the new physics of SS and SiGe materials. Thus, new intrinsic carrier concentration ($n_{i,SS}$) and relative dielectric constant (ε_{SiGe}) of SS and SiGe layer, respectively, were introduced for calculating the Fermi potential (ϕ_f) and transistor body factor (γ) (see eqns. 3 and 4 in [11]). The band-gap dependence of Ge mole fraction (x) can be calculated from the widely accepted semi-empirical SS energy band-gap ($E_{g,SS}$) formula [16]:

$$E_{g,SS} = E_g - 0.4x = 1.11 - 0.4x \quad (eV) \tag{1}$$

The enhancement of low-field electron mobility in the SS layer is described by the new parameter $\mu_{dop,SS}$ that is related with the previous Si mobility parameter ($\mu_{dop,Si}$) by $\mu_{dop,SS} = m \cdot \mu_{dop,Si}$ The enhancement factor m was determined from the empirical mobility data of SS devices reported in [17], where, for example, $m \approx 1.6$ for x=0.15. Note that, in the case of the n-channel SS MOSFET, a single value of m is found to be a good approximation for both low and high gate voltage V_{GS} [17].

It is shown that the impact ionization is dominated in system strained Si/SiGe that silicon, due to band-gap narrowing. Eksperimentalno je pokazano da je udarna jonizacija veća u sistemu napregnuti Si/SiGe nego u slučaju čistog silicijuma pri istim uslovima spoljašnjih polarizacija, što je posledica smanjenja energetskog procepa napregnutog silicijuma. In NQS MOS model, the output drain current I_D in the pre-turn-on region can be expressed as [18]:

$$I_D = \frac{M}{1 - K(M-1)} I_{ch} \tag{2}$$

where I_{ch} is channel saturation current, obtained by NQS MOS sub-circuit, K is the pre-turn-on slope factor. The following **empirical** expression of K versus the effective channel length L_{eff} for SS MOSFET is found $K = k_1 L_{eff}^{k_2}$ (paremeters k_1 and k_2 are given in Table I); M is the well-known avalanche multiplication factor [19]:

$$M = 1 + \frac{A_n l_d E_m}{B_n} \exp\left(-\frac{B_n}{E_m}\right) \tag{3}$$

where:

TABLE I
THE NQS MOS MODEL PARAMETERS OF BULK-SI AND STRAINED-SI/SIGE NMOS TRANSISTORS

Param.	Description	Si MOS	SS MOS
L_{eff}	Channel lenght (μm)	0.1, 0.2, 9.9	0.1, 0.2, 9.9
W	Channel width (μm)	5	5
ΔL	Drain/source – gate overlap length (μm)	0.05	0.05
t_{ox}	Gate oxide thickness (nm)	6	6
x_j	Junction depth (μm)	0.1	0.1
V_{fb}	Flatband voltage (V)	-0.68	-0.94
N_{beff}	Effective channel doping (cm^{-3})	$5 \cdot 10^{17}$	$2.9 \cdot 10^{17}$
μ_{dop}	Doping dependent low-field mobility (cm^2/Vs)	280	476
α	Vertical field mobility degradation factor (V^{-1})	0.33	0.37
v_{sat}	Saturation velocity (cm/s)	$1.206 \cdot 10^7$	$2.29 \cdot 10^7$
β_0	Lateral mobility fitting parametet	1.109	1.109
R_S, R_D	Sorce/Drain resistance (Ω)	140	200
DIBLL	Pre-factor for length dependence of DIBL effect	0.00102	0.000812
DIBLE	Exponent for length dependence of DIBL effect	-2.1	-1.56
VFBLL	Pre-factor for length dependence of flatband voltage (V)	-0.346	-1.08
VFBLE	Exponent for length dependence of flatband voltage (V)	-0.42	0.1
CSLL	Pre-factor for length dependence of body effect	0.46	0.942
CSLE	Exponent for length dependence of body effect	-0.6	-0.105
C	Pre-factor for channel length modulation effect	0.042	0.06
D	Exponent for channel length modulation effect	0.5	0.5
k_1	Pre-factor for K dependence	0.47	0.39
k_2	Exponent for K dependence	-0.43	-0.25
A_n	Impact ionization parameter	$2.45 \cdot 10^5$	$2.84 \cdot 10^5$
B_n	Impact ionization parameter	$1.92 \cdot 10^6$	$3.64 \cdot 10^6$
t_1	Pre-factor for self-heating effect	–	0.045
t_2	Exponent for self-heating effect	–	0.6

$$l_d = 1.7 \cdot 10^{-2} t_{ox}^{1/8} x_j^{1/3} L_{eff}^{1/5} \qquad (4)$$

x_j is pn juntion depth, while A_n and B_n are impact ionization parameters. In eqn. (3), E_m is maximal channel electric field depending of drain voltage V_{DS} as:

$$E_m = \sqrt{\frac{V_{DS}^2}{l_d^2} + \frac{2 E_a V_{DS}}{l_d}} \qquad (5)$$

where E_a include gate voltage V_{GB} and source surface potential ϕ_{S1} dependences:

$$E_a = \frac{q N_B l_d}{\varepsilon_0 \varepsilon_{Si}} - \frac{\left(V_{GB} - V_{fb} - \phi_{S1}\right)}{l_d} \qquad (6)$$

The parameter values with notation and meanings are shown in Table I. They were extracted in the same way as for the case of modelling the bulk-Si devises described in details in [11].

The method of SS NMOSFET model parameter's extraction is identical as in the case of modeling bulk-Si devices [11]. The process-related parameters including effective gate length (L_{eff}), oxide thickness (t_{ox}), and the effective channel doping

(N_{beff}) were known from device geometry and processing. The other parameters, more related with device physics, were found from tuning the simulated and the measured electrical characteristics of several SS devices with various channel lengths. The flat-band voltage parameter (V_{fb}) was extracted from matching the experimental transfer characteristics $I_D - V_{GS}\big|_{V_{DS}=const}$ of the long-channel devices in the sub-threshold region. A theoretical values of velocity saturation parameter (v_{sat}) and the corresponding exponent (β_0), both appearing in the transverse field dependence MOS mobility model, were fine tuned until good match with experimental $I_D - V_{DS}$ output characteristics of short-channel devices around saturation ($V_{DS} \sim V_{Dsat}$) was achieved at high V_{GS}. Namely, in this region, the saturation of output characteristics of short-channel transistors is governed by v_{sat} and not the pinch-off of channel charge. The parameter α, figuring in lateral field dependence mobility models, was evaluated from long-channel $I_D - V_{DS}$ experimental characteristics, aiming to avoid the interference of short-channel effects on the decrease of output conductance. Due to the dominance in short-channel devices, the source/drain ohmic resistances (R_D, R_S) were evaluated from the linear region of $I_D - V_{DS}$

characteristics of short-channel devices. Finally, the only true fitting parameters *DIBLL*, *DIBLE*, *VFBLL*, *VFBLE*, *CSLL* and *CSLE* describing short-channel effects [11] were found from the sub-threshold region of $I_D - V_{GS}$ transfer characteristics of short-channel devices, until a good match was achieved for both low and high constant V_{DS}.

IV. RESULTS

The simulated and the measured transfer and output characteristics of otherwise identical SS MO SFET on 15% Ge virtual substrate and bulk-Si devices with different channel lengths are shown in Figs. 3-5. The characteristics are obtained with using a unified set of NQS MOS model parameters (shown in the table I) for modelling each of the experimental devices.
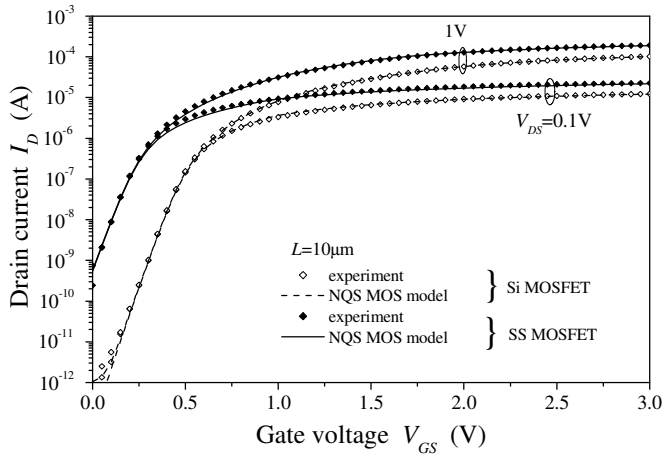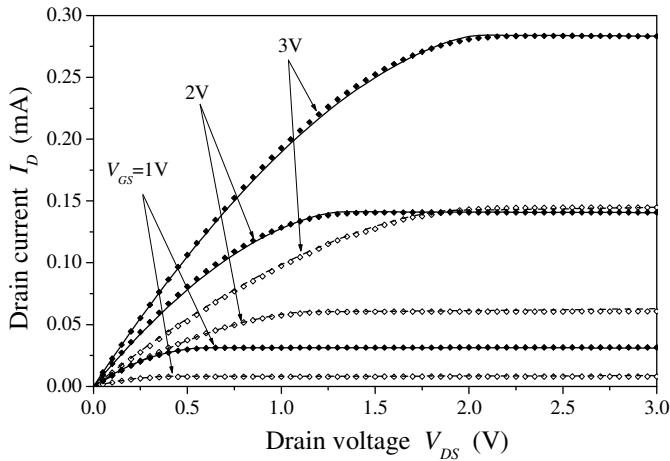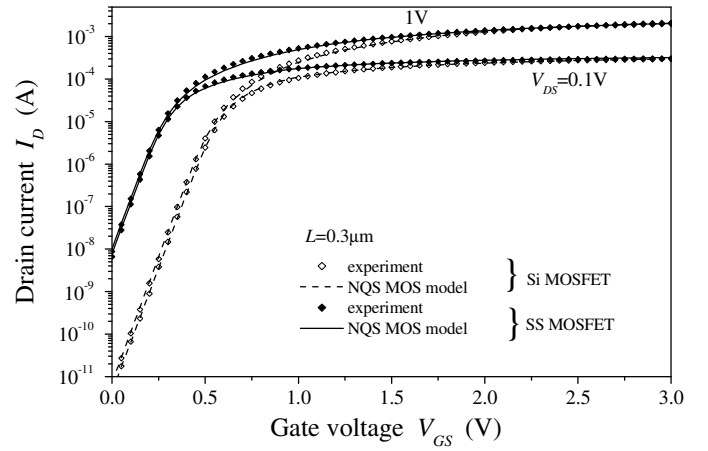

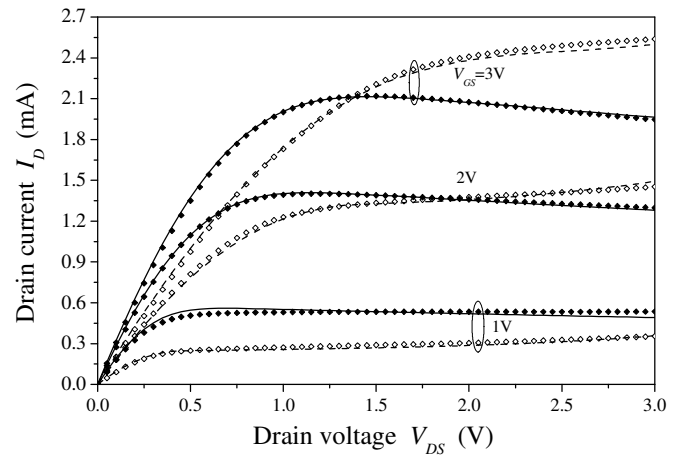Fig. 3. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 10 \mu m$.

Fig. 4. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 0.3 \mu m$.

The DC (or steady-state) self-heating phenomena of MOS devices refer to local increase of channel temperature with dissipating power, that in turn limits maximum device current drive performance. The three main SHEs in NMOSFETS are: a decrease of channel mobility, a drop of threshold voltage and an increase of carrier's saturation velocity. In the higher power dissipative region, however, the mobility degradation predominates all other effects, which subsequently appears as a negative conductance in device output characteristics. SHEs have been incorporated in SS device model through its phenomenological dependence on V_{DS}. Assuming that all SHEs can be summed into one lumped effect of channel mobility degradation, a modified low-field mobility parameter is defined as $\mu^*_{dop,SS} = \mu_{dop,SS} \cdot (1 - t_1 \cdot V_{DS}^{t_2} \cdot L_{eff}^{-1})$, where parameters t_1 and t_2 are given in Table I. From Fig. 4 and Fig. 5, it is seen that the negative output conductance is highly visual in short-channel SS NMOSFETs, whereas the same is not observed in the control Si transistors. However, it is not appeared yet in long-channel SS device characteristics of Fig. 3 due to a substantially lower power dissipation for given

V_{GS}, V_{DS} and because of smaller R_{th} in larger transistors ($R_{th} \sim L^{-1}$). Consequently, since $\mu^*_{dop,SS}$ is less degraded, a current drive enhancement of the SS device over its bulk-Si counterpart is clearly visible for long-channel transistors as shown in Fig. 3. In case of short channel transistors, however, the potential advantage of SS devices is masked by negative conductance and can be revealed in simulations by omitting the SHE model.
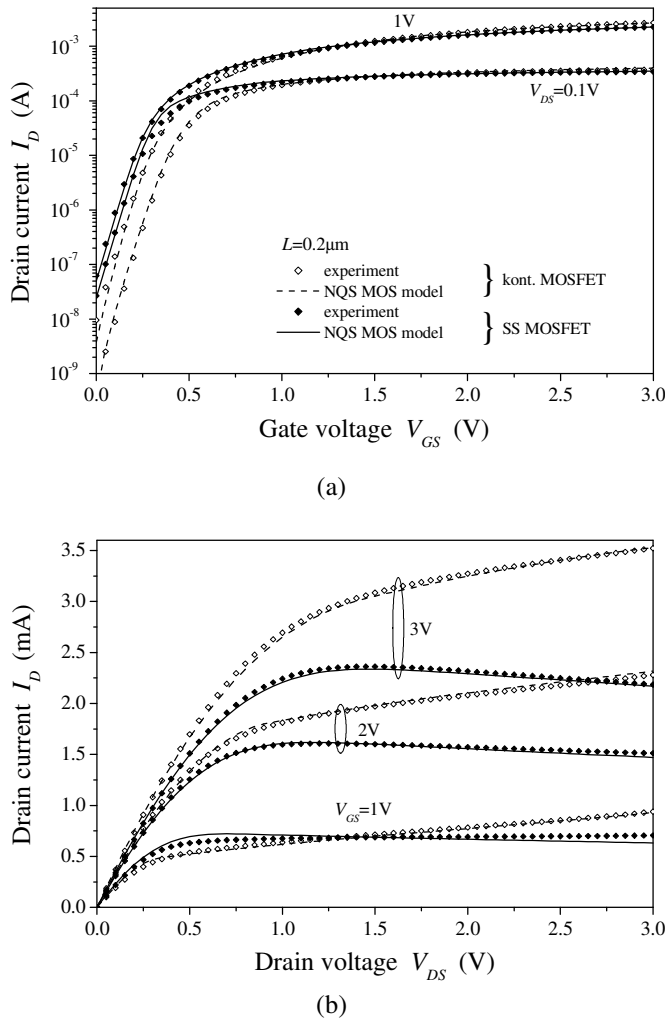
a modified NQS MOS including steady-state self-heating can accurately predict the DC characteristics of strained-Si/SiGe NMOSFETs. It can be also useful for extracting sound physical values of all other model parameters and for realistic estimation of channel mobility enhancement in SS devices beiing marked by the loss of current drive performance due to SHEs.

(a)

(b)

Fig. 5. Transfer (a) and output (b) characteristics of SS MOSFET and control-Si MOSFET with $L = 0.2 \mu m$.

V. CONCLUSION

The bulk-Si NQS MOS device model was successfully modified and implemented for modelling DC characteristics of surface-channel strained-Si NMOSFEs. An efficient method for including the steady-state self-heating effects in the NQS MOS model, which avoids the conventional method of the device temperature extractions with auxiliary subcircuits is also described. From the comparisons of modelling results with numerical simulations and measurements, it is shown that

REFERENCES

[1] A. Dimoulas, E. Gusev, P. Mclntyre, M. Heyns, *Advanced Gate Stacks for High-Mobility Semiconductors*, Springer Berlin Heidelberg, 2007.
[2] C. K. Maiti, L. K. Berra, S. Chattopadhyay, "Strained-Si heterostructure field effect transistors", *Semiconductor Sci. Technology*, vol. 13, pp. 1225-1246, 1998.
[3] M. Currie, "Strained silicon: Engineered substrates and device integration", *Proceedings of 2004 International Conference on Integrated Circuit Design and Technology*, pp. 261-268, 2004.
[4] T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Sugiyama, S.-I. Takagi, "Device Design and Electron Transport Properties of Uniaxially Strained-SOI Tri-Gate nMOSFETs", *IEEE Transactions on Electron Devices*, vol. 55, pp. 649-654, 2008.
[5] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, B. S. Mererson, "Extremely high electron mobility in Si/SiGe modulation-doped heterostructures", *Applied Physics Letters*, vol. 66, pp. 1077-1079, 1995.
[6] Z.-Y. Cheng, M. Currie, C. Leitz, G. Taraschi, E. Fitzgerald, J. Hoyt, D. Antoniadas, "Electron mobility enhancementin strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates", *IEEE Electron Device Letters*, vol. 22, pp. 321-323, 2001.
[7] S. Dhar, H. Kosina, V. Palankovski, S. Ungersboeck, S. Selberherr, "Electron mobility model for strained-Si devices", *IEEE Transactions on Electron Devices*, vol. 52, pp. 527-533, 2005.
[8] J.G. Possum, W. Zhang, "Performance Projections of Scaled CMOS Devices and Circuits with Strained Si-on-SiGe Channels", *IEEE Transactions on Electron Devices*, vol. 50, pp. 1042-1049, 2003.
[9] K. Rim, J. Koyt, J. Gibbons, "Strained Si NMOSFETs for High Performance CMOS Technology", *Proceedings of Symposium on VLSI Technology*, pp. 59-60, 2001.
[10] S.G. Badcock, A.G. O'Neill, E.G. Chester, "Device and Circuit Performace of SiGe/Si MOSFET", *Solid-State Electronics*, vol. 46, pp. 1925-1932, 2002.
[11] T. Pešić, N. Janković, "A compact nonquasi-static MOSFET model based on the equivalent non-linear transmission line", *IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems*, vol. 24, pp. 1550-1561, 2005.
[12] K. Rim, J. Hoyt, J. Gibbons, "Fabrication and analysis of deepsubmicron strained-Si N-MOSFET`s", *IEEE Transactions on Electron Devices*, vol.47, pp. 1406-1415, 2000.
[13] H. Nayfeh, J. Hoyt, D. Antoniadis, "A physically based analytical model for the threshold voltage of strained-Si n-MOSFETs", *IEEE Transactions on Electron Devices*, vol. 51, pp. 2069-2072, 2004.
[14] S. Olsen, A. O`Neill, L. Driscoll, S. Chattopadhyay, K. Kwa, A. Waite, Y. Tang, A. Evans, J. Zhang, "Optimization of alloy composition for high-performance strained-Si-SiGe N-channel MOSFETs", *IEEE Transactions on Electron Devices*, vol. 51, pp. 1156-1163, 2004.
[15] W. Matthews, A. Blakeslee, "Defects in epitaxial multilayers", *Journal of Cryst. Growth*, vol. 27, pp. 118-125, 1974.
[16] R. People, "Physics and applications of Ge_xSi_{1-x} strained-layer heterostructures", *IEEE Journal of Quantum Electronics*, vol. 9. pp. 1696-1707, 1986.
[17] Th. Vogelsang, K. Hofmann, "Electron transport in strained Si layers on $Si_{1-x}Ge_x$ substrates", *Applied Physics Letters*, vol. 63, pp.186-188, 1993.
[18] N. Janković, "Pre-turn-on source bipolar injection in graded NMOST`s", *IEEE Transactions on Electron Devices*, vol. 38, pp. 2527-2530, 1991.
[19] B. Iniguez, T. Fjeldly, "Unified substrate current model for MOSFETs", *Solid-State Electronics*, vol. 41, pp. 87-94, 1996.

Design of Transformer and Power stage of Push-Pull Inverter

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Abstract—**In this paper is presented the example of construction of push-pull inverter that can be used in two different topologies, with two input voltages and three power ratings which can at the same time achieve AVR function and "power-save" feature. Special attention was paid to scheme, turn ratio calculation and transformer coil windings arrangements that with only two types (of different power ratings) allows realization of large number of push-pull inverter configurations that can be applied to different power supply systems.**

Index Terms—**Over-voltage protection, Power stage construction, Push-Pull inverter, Transformer.**

I. INTRODUCTION

S INGLE-PHASE voltage inverters found their wide application in uninterrupted supply systems (UPS) for computers and computer-based devices and recently in power supply systems with renewable energy sources (sun, wind). In both cases inverters play the most important role, which is transformation of DC voltage (usually accumulator battery) to AC voltage that corresponds to power supply. Basic requirements for the devices that are used with such delicate application are: simplicity, reliability, efficiency and low price.

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In cases when input DC voltage is low (12/24 V), and required inverter power relatively high (several kVA), the above mentioned requirements in both applications are satisfied to great extent typologies of push-pull (PP) inverters and two parallel push-pull (2PP) inverters with secondary transformers serially connected because of low number of components and low conduction losses. Output voltage of such inverters often has so-called "modified/quasi-sinus" wave shape that allows further increase in efficiency (minimum switch losses) as well as control according to the proposed criteria (usually regulation of effective value with required precision). [1]

Standard requirements for construction of power stage of inverter are: compactness, small dimensions, low weight, simple assembly and service. Besides these requirements there was a request that construction solution of inverter should be in such manner that both interest typologies (PP and 2PP) can be realized with simple configuration, that three typical power ratings can be achieved (0.5, 1 and 2 kVA) for input voltages 12/24 V, with the ability to achieve several variants of AVR (*Automatis Voltage Regulation*) function and "power save feature". [2] [3] [4] [6]

Because of its crucial importance for accomplishment of the above mentioned functions and its great influence on achieving the optimal constructing solution, special attention was devoted to the choice of scheme and calculation of transformer parameters. After the detailed analysis variant of transformer with eight windings and two power ratings (0.5 kVA (S_{500}) and 1 kVA (S_{1000})) was suggested. It allows all the interest variants of the device and it fits perfectly to the construction solution. [11].

II. INVERTER OUTPUT VOLTAGE

"Quasi-sinus" wave shape was chosen for inverter output voltage because it fully satisfies target consumers (computers and household devices), it allows minimal switch losses and it also allows control based on different criteria (minimal THD, basic parameters are the same as in the corresponding sinus signal, effective value is constant). Topologies PP and 2PP are shown in *Fig.* 1 and they are suitable for formation of voltage with "quasi-sinus" wave shape. Specificity of the presented PP inverter (*a*) is in the added reset winding of the transformer (n_d) and power semiconductors switches (T_3, T_4) which are necessary for formation of the required output voltage wave shape. With 2PP topology (*b*) "quasi-sinus" output voltage is achieved through voltage time shifts of individual PP inverters. Control was chosen according to the criteria that

inverter output voltage effective value ($U_{o.ef}$) is constant, with limitation that impulse width(t_u) is always greater than certain minimal value ($t_u \geq T/4$), *Fig.* 2. [11].

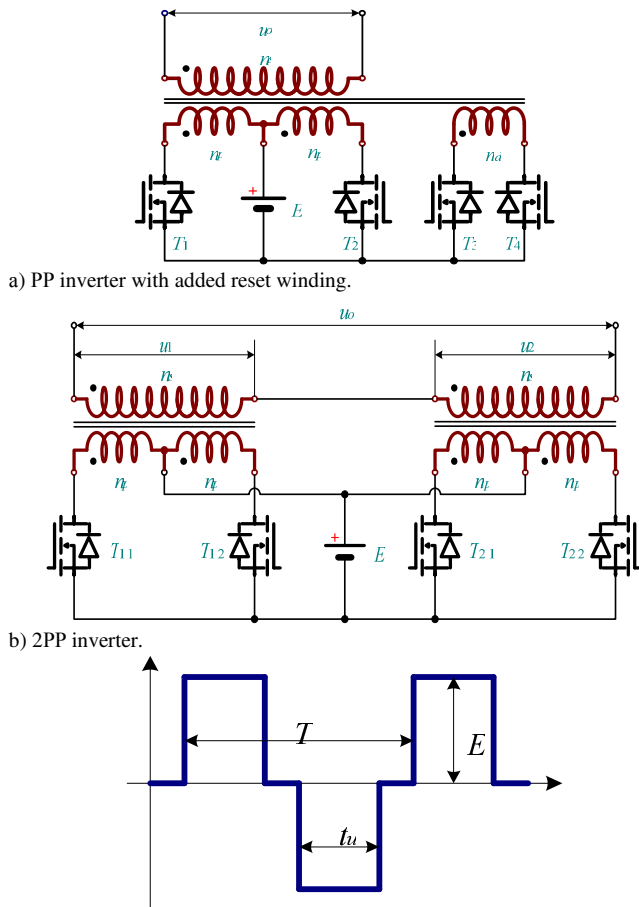a) PP inverter with added reset winding.

b) 2PP inverter.

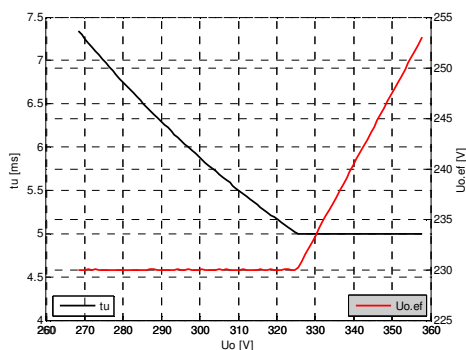Fig. 1. c) Inverter output voltage.

Fig. 2. Dependance of $U_{o.ef}$ i t_u from changes in secondary voltage for $t_u \geq T/4$.

As a consequence to the above mentioned limitation, in certain areas of change in input voltages there is no regulation of effective value of output voltage. In order to reduce that area we can influence it by the choice of working point used for calculating transformer turn ratio.

In other words, the choice of secondary voltage maximum value. If maximum value of transformer secondary voltage corresponds to the maximum voltage of accumulator (approx. 2.4 V/cell), problem of unregulated effective value is being mitigated because operating accumulator voltage/secondary voltage is significantly lower than the maximum, so it does not reach deeply into the restriction area t_u. When the maximum

value of secondary voltage corresponds to accumulator maintenance voltage (approx. 2.3 V/cell), restriction period t_u is longer, and so the divergence of output voltage effective value is greater. The highest effective value is in any case within limitations from 1.1 $U_{o.ef.nom}$.

III. CONSTRUCTION OF INVERTER POWER STAGE

Satisfaction of construction terms demanded detailed analysis and calculation of all the components of the power stage as well as the methods and procedures required for the achievement of the optimal solution.

A. Establishment of connections between power components

One of the most important decisions in the construction of inverter power components is component assembly procedure or integration level. Our experience [6], but also manufacturer's experience [7] suggests that the base for construction should be double-sided printed circuit board (PCB) that is also used as component carrier, primarily for cooler, and medium for establishment of all electrical links between the components of the executive body.

PCB allows that the links between components are established in such manner that all the ways of current commutations are the shortest possible. Besides that, all the components that are necessary for switching on/off and protection of power switches can be positioned in the closest vicinity of the switches that additionally simplifies the assembly and increases reliability of the device. Besides the semi-conductive components and components necessary for AVR function and power save, it is also possible to place circuit and voltage measuring transformers and matching fuses on PCB. In that manner, the number of necessary conductors/wires is minimized, assembly of the power stage and its connecting to other device components is simplified to the maximum level and it can be performed by labor force with minimum expertise. Electrical and mechanical/ construction features of the device are improved, reliability is enhanced and cost is lowered.

PCB use for realization of inverter power stage also brings certain limitations. Because of its mechanical characteristics (flexibility, capacity) it is agreed that dimensions of PCB should not exceed 160x240 mm. Second serious limitation is maximum value of current that can be transmitted through printed connections. For the safety and reliability reasons and with regard to the available width of the connections it is estimated that total current in one PP should be limited to 50 A. It disabled the application of certain converter types at lower voltage and with greater power, mostly PP at 12 V. 2PP can be applied in all cases because of splitting of input power, except for 12 V, 2 kVA (*Table* 1.).

B. Choice, protection and triggering the switch

Choice of semi-conductive power switches and their security and triggering manner has crucial influence on operating quality, reliability and efficiency of the inverter. For the sake of simplicity, switches are represented as single components on the inverter schemes (*Fig.* 1.), but in reality each one consists of parallel link of up to four MOSFET in TO220 case.

TABLE I
MAXIMUM CURRENT OF POWER SWITCH

$U_{Bat.nom}$ [V]	12						24					
Power [kVA]	0.5		1		2		0.5		1		2	
Topology	PP	2PP	PP	2PP	PP	2PP	PP	2PP	PP	2PP	PP	2PP
$I_{prek.max}$ [A]	50	25	100	50	200	100	25	12.5	50	25	100	50

Such configuration is completely satisfactory in its technical characteristics, price and dimensions [7].

Electrical current values for two input DS voltages, three power ratings and two inverter topologies are provided in *Table* 1. Currents are calculated for minimum input voltage and numbers are rounded. Fields in which current exceeds maximum values (50 A) are marked.

Several popular and available MOSFET types that can be used as components of power switch with acceptable price are listed below. Basic characteristics are provided for each type. 100 V MOSFET are chosen because they can be applied to both operating voltages. [10]

- IRF540N: V_{DS}=100 V,
  I_D=33 A/25 °C; 23 A/100 °C,
  I_{Dpulse}=110 A,
  R_{DSon}=44 mΩ/25 °C; 70 mΩ /80 °C,

- IRF3710: V_{DS}=100 V,
  I_D=57 A/25 °C; 40 A/100 °C,
  I_{Dpulse}=230 A,
  R_{DSon}=23 mΩ/25 °C; 35 mΩ /80 °C,

- SPP70N10L: V_{DS}=100 V,
  I_D=70 A/25 °C; 50 A/100 °C,
  I_{Dpulse}=280 A,
  R_{DSon}=16 mΩ/25 °C; 20 mΩ /80 °C.

In order to achieve full reliability power switches should be over-dimensioned to reasonable extent. That means that components that can endure current pulling caused by transformer magnetization and capacitor charging, giving the values that are several times greater than nominal currents. We can see in the MOSFET characteristics that they can endure impulse currents four times greater than prescribed values. Since every switch has up to 4 MOSFET, fulfilling that condition is very simple.

Over-current protection of the power switches is realized by measuring of output current with transformer (part of power stage) and reduction of output voltages estimated value.

Natural voltage doubling and voltage peaks that cause inevitable parasite components ask for careful choice and calculation of over-voltage protection of PP inverter switch. The first procedure in establishment of the high quality over-voltage protection is the construction procedure and it consists of reducing the extent of parasite components to the lowest possible level and minimization of computational current loops (preventing over-voltage from occurring). With bridge converters this procedure is in most cases sufficient if it is performed in the correct manner, but with PP converters total elimination of over-voltage is not possible on switches if we apply only the construction methods. That means that we have to use some other methods. Use of some of the passive protections (RC, RCD) makes the construction more complicated, it brings in the additional losses and it reduces reliability of the device (larger number of the components), and it also requires complicated calculations with experimental determination of certain parameters. For that reason, in our specific case, active over-voltage protection was used that at the same time protects all the switches in PP with constant voltage follow-up at their drains (ports $D_{h.1}$, $D_{h.2}$), in relation to the power supply voltage (port +*S*) (*Fig.* 1.) [11]. If the voltage between any drain and input voltage is greater than the prescribed one, protection enables both power switches and it released all the accumulated magnetic energy that caused over-voltage. In that manner the protection only follows voltage on the switches and they, through the change in the guidance manner protect themselves. This protection consists of several signal transistors and diodes as well as low power resistors (0.25 W) (*Fig.* 3.), so this is very cheap solution with practically no dissipation and that can be easily placed on the PCB of the inverter power stage next to the power switches that it protects.

It is planned that switching on/off of the power switches is made possible with standard circuit IR2110 [10] (*Fig.* 3.), which controls both PP inverter switches, and it can be conveniently adjusted to over-voltage protection operating and placed on PCB next to the power switches.
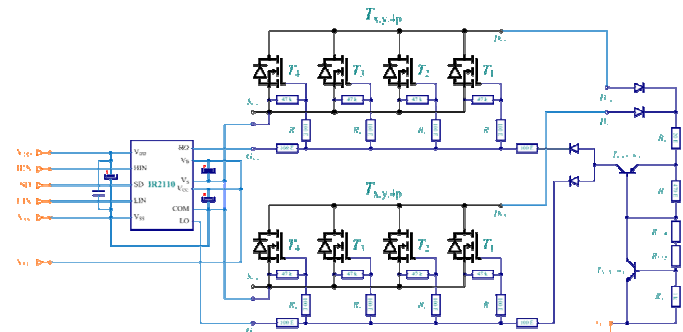

Fig. 3. Triggering of power switches and over-voltage protection.

C. Cooling of the power stage components

The simplest assembly solution is the power stage alternative in which all four power switches (with up to four individual MOSFET) are placed on individual, galvanic ally separated heat sinks. Application of PCB for establishment of connections between power components in the power stage lead to the limitation of the space available for the placement of heat sinks. For that reason forced cooling with standard ventilators (12/24 V) was selected, and it includes thermal switches (70-80 °C). Additional reason for the use of forced cooling was also the demand that the heat sink profile should be the simplest possible and with as little mechanical processing as possible, because of lowering the costs of entire device. Ability of the selected MOSFET types to conduct maximum current, and that the power drop remains minimal in

them [10] (minimal conduction losses), as well as minimal switch losses (low operating frequency and non-existence of over-voltage in switch turning off) made total losses on switches low, so cheap heat sinks with small dimensions and simple profile could satisfy the demands for adequate cooling.

D. AVR function

Important SBN part with which sensitive consumers are supplied through inverter/accumulator battery only when voltage in the mains power system is out of stated boundaries (*off-line*), and which can significantly improve their operating quality is so called AVR function. It is a circuit that fixes voltage in the mains power system and in that manner it expands the scope of input voltages for which the inverter does not have to be switched on (battery use). It is possible to increase and decrease the voltage in one or more steps. AVR principle is demonstrated in *Fig. 4*.
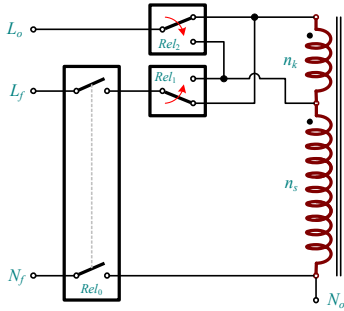

Fig. 4. Basic principle of AVR function (1+1).

Voltage from the mains power system (u_L) is brought between the ports L_f and N_f, and output voltage (u_o) is between L_o and N_o. Transformer consists of the basic (n_s) and correction winding (n_k). Correction of mains power supply is achieved by corresponding switching on/off of relay Rel_1 and Rel_2. Relay Rel_o separates mains system from the rest of device during inverter operating time and it allows realization of power save feature.

- When mains power system voltage is within the boundaries ($u_{L=}$) both relays are switched off and input voltage is equal to output voltage.
- If mains power system voltage is greater ($u_{L>}$), relay Rel_1 is switched off and Rel_2 is switched on. Output voltage is then equal to:

$$u_o = \frac{n_s}{n_s + n_k} u_L = k_{k.sp} \cdot u_L ,$$ (1)

and it is lower than input voltage.
- In case that mains power system voltage is lower ($u_{L<}$), relay Rel_1 is switched on, and Rel_2 is switched off. Output voltage is greater than input voltage:

$$u_o = \frac{n_s + n_k}{n_s} u_L = k_{k.po} \cdot u_L .$$ (2)

- If mains power system voltage is out of boundaries in which its correction is possible ($u_{L<>}$), relay Rel_o is switching off and the device turns to inverter mode.

Specificity of the presented AVR concept is the use of single correction winding for both increasing and decreasing the voltage, which makes the scope boundaries asymmetrical.

AVR output voltage should be in the following scope:

$$u_o \in [k_{pod} \cdot U_{L.ef.nom} - k_{pre} \cdot U_{L.ef.nom}]$$ (3)

- k_{pod}=0.9,
- k_{pre}=1.1,
- $U_{Lef.nom}$=220/230 V.

Maximum voltage increase coefficient:

$$k_{k.po.max} = \frac{k_{pre}}{k_{pod}} = \frac{1.1}{0.9} = 1.222 ,$$ (4)

is determined in such manner that in case that voltage increase is turned on with $u_L = k_{pod} \cdot U_{L.ef.nom}$ (greatest input voltage in which the voltage increase feature can be turned on) output voltage is not greater than $k_{pre} \cdot U_{L.ef.nom}$. Corrector winding has to have less than or equal number of windings than: (2)(3)

$$n_{k.max} = \left(\frac{k_{pre}}{k_{pod}} - 1 \right) \cdot n_s = \left(\frac{1.1}{0.9} - 1 \right) \cdot n_s = 0.222 \cdot n_s .$$ (5)

Minimum and maximum input voltage for which output voltage is satisfactory is: (3)

$$U_{L.MIN} = \frac{k_{pod}^2 \cdot U_{L.ef.nom}}{k_{pre}} = 0.736363 \cdot U_{L.ef.nom} = 169.4_{230} \text{ V} ,$$ (6)

$$U_{L.MAX} = \frac{k_{pre}^2 \cdot U_{L.ef.nom}}{k_{pod}} = 1.3444 \cdot U_{L.ef.nom} = 309.2_{230} \text{ V} .$$ (7)

It is evident from the analysis that it is possible to make AVR (1+1) (1 increase feature and 1 decrease feature) that in wide range of input voltage change $[U_{L.MIN} - U_{L.MAX}]$ provides satisfactory output voltage. (3)

It is not common to operate in such wide range of input voltage in practice, so in regular use there is correction winding in which $n_k < n_{k.max}$. In that manner creation of transformer is simplified, possible difficulties with output voltage are avoided and the range of tolerable change in input voltage remains sufficiently wide. For the calculation of correction winding we set a condition that in $u_L = k_{pod} \cdot U_{L.ef.nom}$, AVR output voltage is equal to $U_{L.ef.nom}$. From the provided condition we can draw the following:

$$k_{k.po} = \frac{1}{k_{pod}} = \frac{1}{0.9} = 1.111 ,$$ (8)

$$n_k = \left(\frac{1}{k_{pod}} - 1 \right) \cdot n_s = \left(\frac{1}{0.9} - 1 \right) \cdot n_s = 0.111 \cdot n_s .$$ (9)

$$U_{L.MIN} = k_{pod}^2 \cdot U_{L.ef.nom} = 0.81 \cdot U_{L.ef.nom} = 186.3_{230} \text{ V} ,$$ (10)

$$U_{L.MAX} = \frac{k_{pre} \cdot U_{L.ef.nom}}{k_{pod}} = 1.2222 \cdot U_{L.ef.nom} = 281.1_{230} \text{ V} \quad (11)$$

If we add another correction winding we can also achieve functions (2+1) (2 levels of increase and 1 decrease) and (2+2) (2 levels increase and 2 decrease). (Case (1+2) (1 level increase, 2 decrease) is not interesting in practice). Larger number of windings and relays means more possibilities for adjustment of input voltage. Because of simplified construction, lowered demand for control electronics and simplification and lowering the cost of the device we have chosen the AVR (1+1) alternative which through single added winding and two relays adjusts changes in input voltage in sufficiently wide range. (6) (7) [11].

E. Power save feature

Efficiency of the device is crucial in case of power supply from accumulator battery, especially if it is charged from renewable source (wind, sun). One of the methods to increase efficiency is so called power save feature. It is the capability of inverter to recognize idle mode or operating under minimal load and in that case it should automatically turn off. Besides that, inverter has to automatically turn on when overload occurs again. Besides significant power save, this feature increases the handling commodity (it is not necessary to turn it on and off, only to hook or remove load). For realization of this feature, besides the relays on the PCB, some adequate circuits are necessary in the control electronics. [11].

F. Electrical schematics

On *Fig.* 5. is provided electrical schematics of entire power part of the inverter which represents maximum variant necessary for achievement of all configurations of the device through the adequate choice of active components.

IV. DESIGN OF PP INVERTER TRANSFORMER

In order to achieve two inverter topologies with two levels of input voltage, three power ratings, with or without AVR, it is theoretically necessary to have 48 different types of transformers. If we use only AVR (1+1) in PP for the practical reasons (there is already one added winding), number of necessary transformer types reduces to 30. When we add the restriction that input current should not be greater than 50 A, which is a consequence of construction design (power stage on PCB), we are left with 16 transformer types which is still a large number for production.

For that reason analysis was conducted and it aimed search for configuration that could make possible the realization of all interest variants of the device through the use of minimal number of different transformer types. Analysis result is provided in *Fig.* 6. It is a transformer with eight windings and with the correct arrangement of the windings it is possible to realize all the variants of the inverter with only two powers: 0.5 kVA (S_{500}) and 1 kVA (S_{1000}). [11]
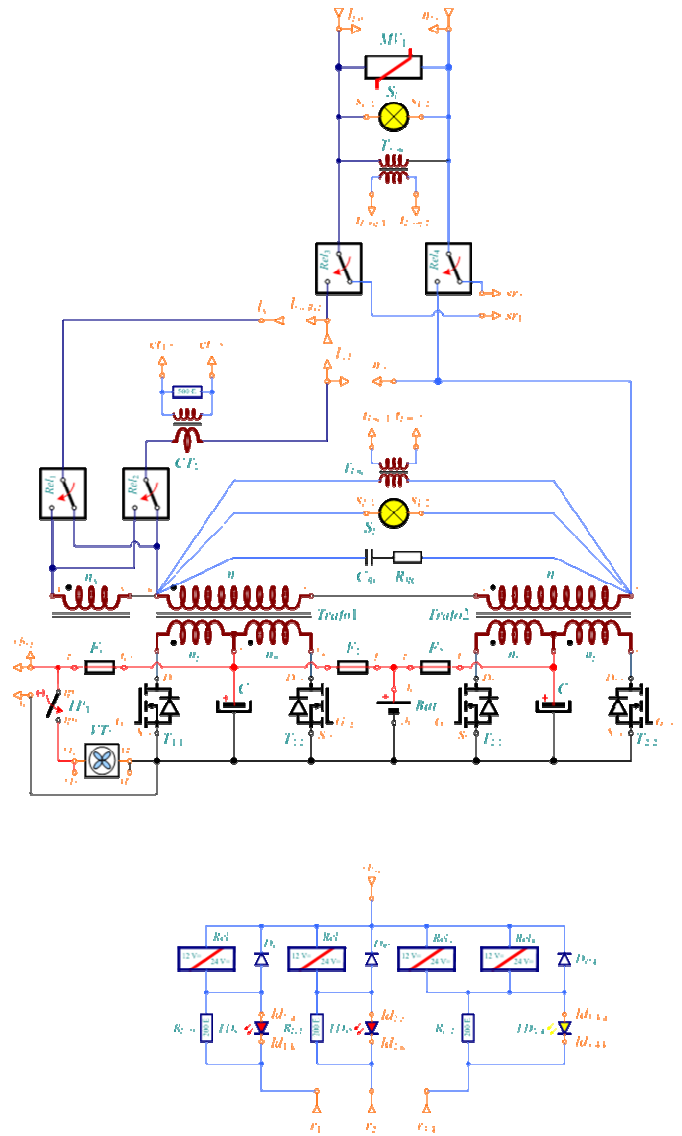

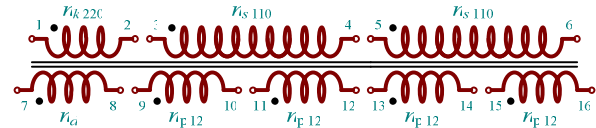Fig. 5. Electrical schematics of inverter power stage.

Fig. 6. PP inverter transformer-general case.

- Four primary windings $n_{p.12}$ (ports 9-10, 11-12, 13-14, 15-16) have the number of windings that corresponds to input DC voltage (12V), and wire cross-section area (CSA) that corresponds to current that would, for the given power, run through the windings with input DC voltage 24 V.

- Two secondary windings $n_{s.110}$ (ports 3-4, 5-6) have half of the number of windings that corresponds to the necessary inverter output voltage. Wire CSA for their winding is determined according to current that would run through the windings for provided power and AC voltage 220/230 V (on both windings).

- Added correction winding $n_{k.220}$ (ports 1-2) has to have 11 % of total number of windings (2 $n_{s.110}$) and wire CSA as $n_{s.110}$.

- Additional correction winding, or magnetic energy reset winding n_d (ports 7-8), has to have the same number of windings and wire CSA as $n_{k.220}$.

A. Transformer turn ratio calculation

With regard to PP inverter function, its operating principles and manner of output voltage regulation, as well as type of load (computers, lighting etc.), transformer turn ratio should be chosen in such manner that consumer never experiences voltage higher than maximum allowed ($U_{L.ef.nom}$ $\sqrt{2} \cdot k_{pre} = 358_{230.1.1}$ V).

$$U_{sek.MAX} = U_{prim.MAX}\, 2PO_I = U_{L.ef.nom}\sqrt{2}k_{pre} = 358\,\text{V} . \quad (12)$$

Maximum and minimum primary voltages of the transformer are: [11]

$$U_{prim.MAX} = U_{bat.max} - U_{DS.min}(I_{min}, \Theta_{min}) \approx 14/28 \text{ V} . \quad (14)$$

$$U_{prim.MIN} = U_{bat.min} - U_{DS.max}(I_{max}, \Theta_{max}) \approx 10.4/20.8 \text{ V} \quad (15)$$

- U_{DS}, $I_{min/max}$: transistor voltage, current,
- $\Theta_{min/max}$: operating temperature.

Now the transformer turn ratio is: [11]

$$PO_I = \frac{U_{sek.MAX}}{U_{prim.MAX}} = \frac{n_{s.110}}{n_{p.12}} \approx 13 . \quad (16)$$

It is necessary to check whether the calculated turn ratio is satisfactory even in cases when mains power system voltage is present in secondary windings. Maximum voltage that occurs in the primary windings always has to be lower than maintenance voltage of accumulator battery, otherwise it would have negative impact on its charging (through diodes of power MOSFET switches), because it is performed by independent charger.

$$U_{prim.MAX} \cdot \sqrt{2} - V_D = \frac{U_{sek.MAX} \cdot k_{pre}}{2 \cdot PO_I} - V_D \approx 13/26.8\,\text{V} , \quad (17)$$

this condition is also fulfilled.

B. Transformer winding arrangement

Examples of transformer winding arrangements for several configurations and inverter types are provided in *Fig. 7*.

C. Practical realization of transformer

Example of practical realization of type transformer, 1 kVA power, winded according to scheme provided in *Fig.* 6. And with windings according to the provided calculation is shown in *Fig.* 8. it is a compact solution with which is possible to get all the interesting variants of inverters with 1 and 2 kVA powers through simple adjustments.
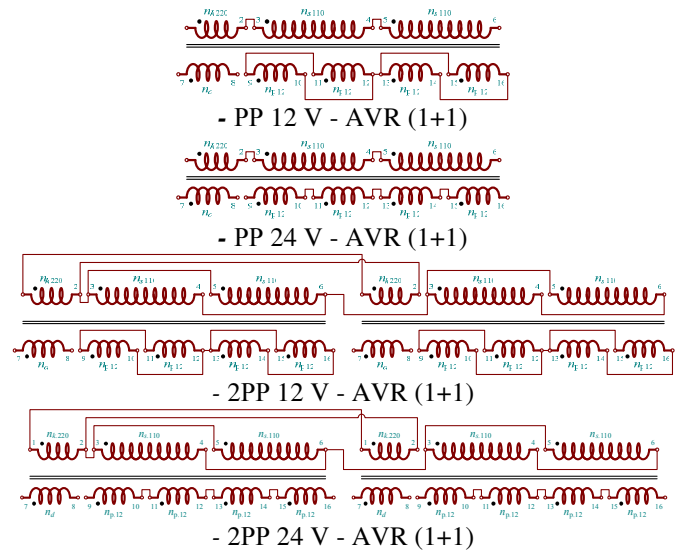

- PP 12 V - AVR (1+1)

- PP 24 V - AVR (1+1)

- 2PP 12 V - AVR (1+1)

- 2PP 24 V - AVR (1+1)

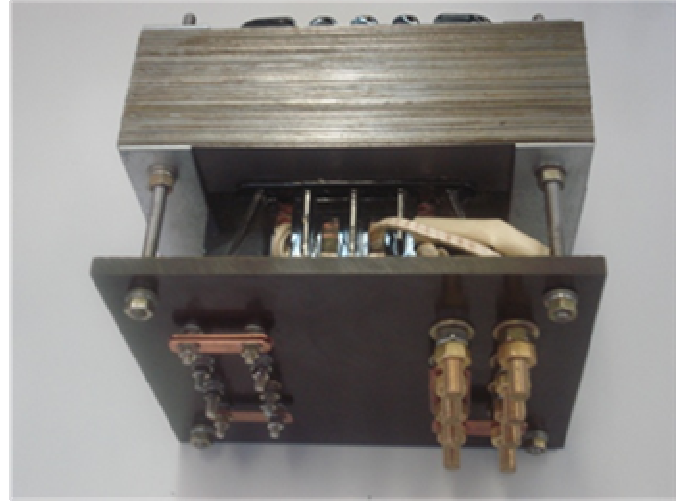Fig. 7. PP inverter transformer-winding arrangement examples.

Fig. 8. PP Inverter transformer-practical realization.

V. 2PP INVERTER 24 V/ 2 KVA

Example of practical realization of 2PP inverter on PCB is provided in Fig. 9. It is evident that it is simple and cheap construction solution with high integration level and increased reliability. The demonstrated compact module is possible to assemble in vertical or horizontal position, in different cases, and to simply connect it to other inverter components (control electronics module, power transformer(s), battery, etc.)

On *Fig. 10.* is presented 2PP inverter 24 V/ 2 kVA (prototype), realized through the compact power stage on PCB and type transformer 1 kVA, which is part of power supply system from renewable source (solar panel+battery).

Fig. 9. Compact inverter power stage on PCB.

Fig. 10. Compact inverter-prototype.

VI. CONCLUSION

Conducted analysis and presented results show that it is possible to achieve significant improvements of the power stage in PP inverter through the use of PCB. Three power ratings of inverter were realized (0.5, 1 and 2 kVA) depending on input battery voltage (12/24 V) and converter type (PP, 2PP). for greater powers, 3-10 kVA, it is necessary to establish some of the links on copper plates, which increases power capacity of inverter power stage and therefore output power also increases. Further improvements of this class of inverters would be aimed towards integration of control electronics and power stage on PCB in order to gain further compactness, reliability and assembly simplicity of such devices.

REFERENCES

[1]   W.G. Gfrorer: "*Power Inverters* 12 V *to* 230 V*"*, 2002.
[2]   D. Jokić, M. Šoja, S. Lubura: „*Naponski invertor veće snage, napajan sa* 12 (24) V$_{DC}$", INFOTEH-JAHORINA, Vol. 5, Ref. E-IV-3, p. 449-452, March 2006.
[3]   D. Jokić, M. Šoja: „*Naponski invertor realizovan sa dva puš-pul pretvarača u paralelnom radu*", INFOTEH-JAHORINA, Vol. 6, Ref. E-VI-16, p. 611-614, March 2007.
[4]   Advanced Solar Product Ag, *Top Class Manual*, 02/2003.
[5]   Steca, *Solar Electronic Product Catalogue*, 2005/2006.
[6]   K-INEL, *Tehnička dokumentacija*, 2006-2008.
[7]   www.apc.com, jun 2008.
[8]   www.stecasolar.com, jun 2008.
[9]   www.greenpower4less.com, jun 2008.
[10] www.ir.com, jun 2008.
[11] B. Dokić, M. Šoja, S. Lubura: „*Izvještaj o stepenu realizaciji naučnoistraživačkog projekta...Ugovor broj*:0660-020/961-52/07", jul 2008.

Why does the grid needs cryptography?

V. B. Litovski, P. M. Petković

Abstract—**New developments and the future of electrical energy production and distribution system are investigated first. Use of alternative energy resources, synergy with the existing large energy generation facilities, control of the distribution, integrated billing and control, information distribution via the grid and many others are the facts that are to be considered while conceiving the system in future. It comes that electronics and ICT will play a major role in control, billing and communication. Information is expected to flow at any level of distribution and control. That already gives opportunities for misuses such as tampering and eavesdropping at the power lines used for communication imposes the need of secure communication. We will, therefore, explain how and why cryptography is intended to be used within the TR 1107 project (financed by the Serbian Ministry of Science) in order to prevent attacks on the information distributed via the grid. We also discuss the physical implementation of the cryptographic infrastructure with special attention paid to the so-called side channel attacks (SCA).**

Index Terms—**Electricity, control, grid, microgrid, tampering, eavesdropping, cryptography, side channel attack.**

I. INTRODUCTION

MODERN society critically depends on a secure supply of high-quality electrical energy [1].

According to an International Energy Agency estimate, global investments required in the energy sector over period 2003-2030 are about USD 16 trillion. Future electricity grids have to adapt to changes in technology while matching societal values for environment and commerce. Technologies should also demonstrate reliability, sustainability, and cost effectiveness.

At the distribution level, the new requirements call for the development of:

- distribution grids accessible to distributed generation (DG) and renewable energy sources (RESs), either self-dispatched or dispatched by local distribution system operators,
- distribution grids enabling local energy demand management interacting with the users through smart metering systems, and
- distribution grids that benefit transmission dynamic control techniques and overall level of power security, quality, reliability, and availability.

Putting all together, distribution grids are being transformed from passive to active networks in the sense that decision-making and control is distributed and the power flows bi-directionally. The function of the active distribution network is
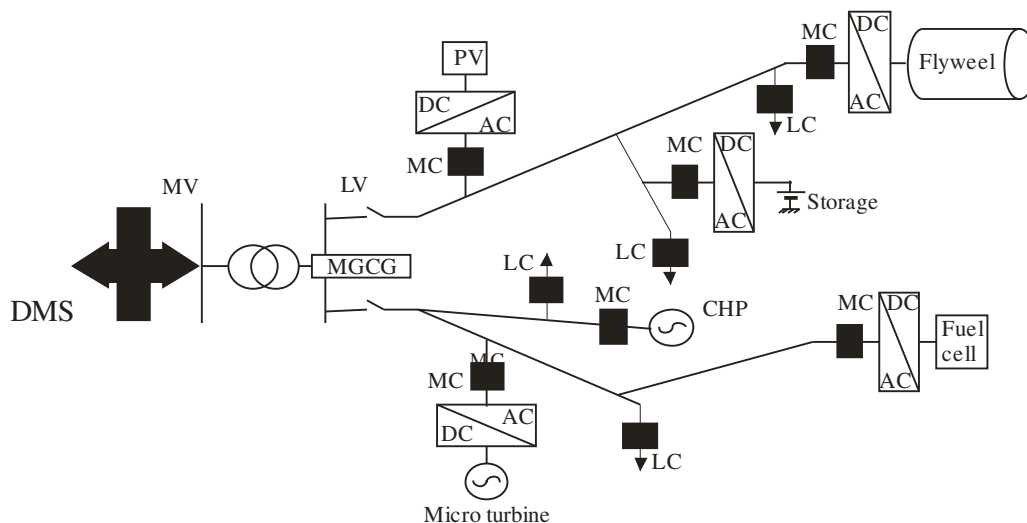

Fig. 1. Typical microgrid structure coordinated by the *microgrid central controller* (MGCC) and interfaced to the *distribution management system* (DMS) [MV = medium voltage, LV = low voltage, MC = medium current, PV = photo voltaic, LC = low current, CHP = combined heat and power] [1].

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to efficiently link power sources with customer demands, allowing both to decide how best to operate in real time. Power flow assessment, voltage control, and protection require cost-competitive technologies and new communication systems with information and communication technologies

(ICTs) playing a key role.

Probably the most promising novel network structure is the microgrid paradigm. Microgrids comprise low voltage (LV) distribution system with distributed energy resources (DERs) as shown in Fig. 1, offering considerable control capabilities over the network operation. These systems are interconnected to medium voltage (MV) distribution network, but they can also operate isolated from the main grid in case of faults in the upstream network.

To demonstrate the importance of the communication part of the microgrid-to-utility grid interconnection one may analyze Fig. 2 [2] where a schematic diagram of the interconnection switch based on circuit breaker is shown. Information is distributed both inner to the microgrid, and upstream to the utility network. Real time monitoring and inter-utility information sharing is handled. In that way control (voltage, frequency, power factor etc.) is enabled while, in parallel, the billing system and communication is made possible.
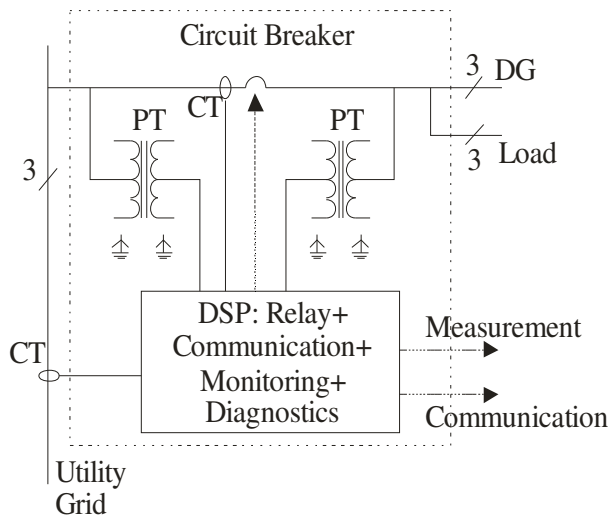

Fig. 2. A circuit breaker based interconnection switch.

Fig. 3 emphasizes another view to importance of the ICTs for the future of the distribution system [3]. On one side it represents a bit futuristic view of a "household" where all loads and the advanced metering device are informatically interconnected to a dashboard that is controlled by the customer. It is supposed the customer will be capacitated to control the use of the resources that were made available to him based on information (measurement, billing, and pricing data) gathered at the dashboard. In the same time all customers are informatically interconnected to the "Meter Data Management Agency" and indirectly to the "Independent System Operator". This is to anticipate a steady progression toward a Participatory Network.

An "advanced meter" (a collection of which is known as an Advanced Meter Infrastructure, or AMI) is an electronic meter that can be read and controlled remotely. In Fig. 3. we show how an AMI network could be organized in the future [3]. The network is divided into three main domains that are connected via Field-Area-Network (FAN) and potentially Wide-Area-Network (WAN) links.

Meters today already provide many potential advantages to ESPs, their customers, and many other entities:

1) *Customer control*: Customers gain access to information on their current energy usage and real-time electricity prices.

2) *Demand response*: Power utilities can more effectively send control signals to advanced metering systems to curtail customer loads, either directly or in cooperation with the customer's building automation system. Current demand response schemes are typically very coarse-grained and provide marginal power savings.

3) *Improved reliability*: More agile demand response and DER management can improve the reliability of the distribution grid by preventing line congestion and generation overloads. These improvements will also reduce the strain on the transmission grid.

4) *Simplified sub-metering*: a single meter can monitor multiple customers, reducing equipment costs and maintenance burdens.

There are several distinct categories of advanced metering systems that support the functionality discussed above with varying degrees of success. The least capable systems use low-bandwidth, time-multiplexed radio networks, which preclude any advanced functionality beyond simply reading the meters due to bandwidth limitations. More capable systems use mesh networks to provide more consistent and perhaps higher-bandwidth connectivity, and the most capable systems have full broadband network connections. The less capable systems are typically less expensive to deploy initially, but high-bandwidth systems support more advanced services, possibly providing more economic benefits in the long run.

This was all to enable the envisagement of the complexity of the information infrastructure needed for the establishment of the future distribution system. There is an international push toward a more advanced infrastructure for the metering of electrical usage [4]. This is driven by applications like demand response, distributed energy resources, outage management, prepayment schemes, and improved theft detection as well as a desire to eliminate the expense of manually reading the meters in the field. AMI aims to accomplish this with computer-controlled meters linked by digital networks [5, 6].

In the next threats to the AMI system conceived above will be considered first. Then, a view of an ICT infrastructure will be analyzed in order to come to the right physical position of the conceived cryptographic chip planned to be developed at the LEDA laboratory. Design requirements will be discussed in order to get the right functionality and SCA resistance. In the appendix we are presenting a simplified version of the public key cryptography procedure in order to give some basic insight in the technology.
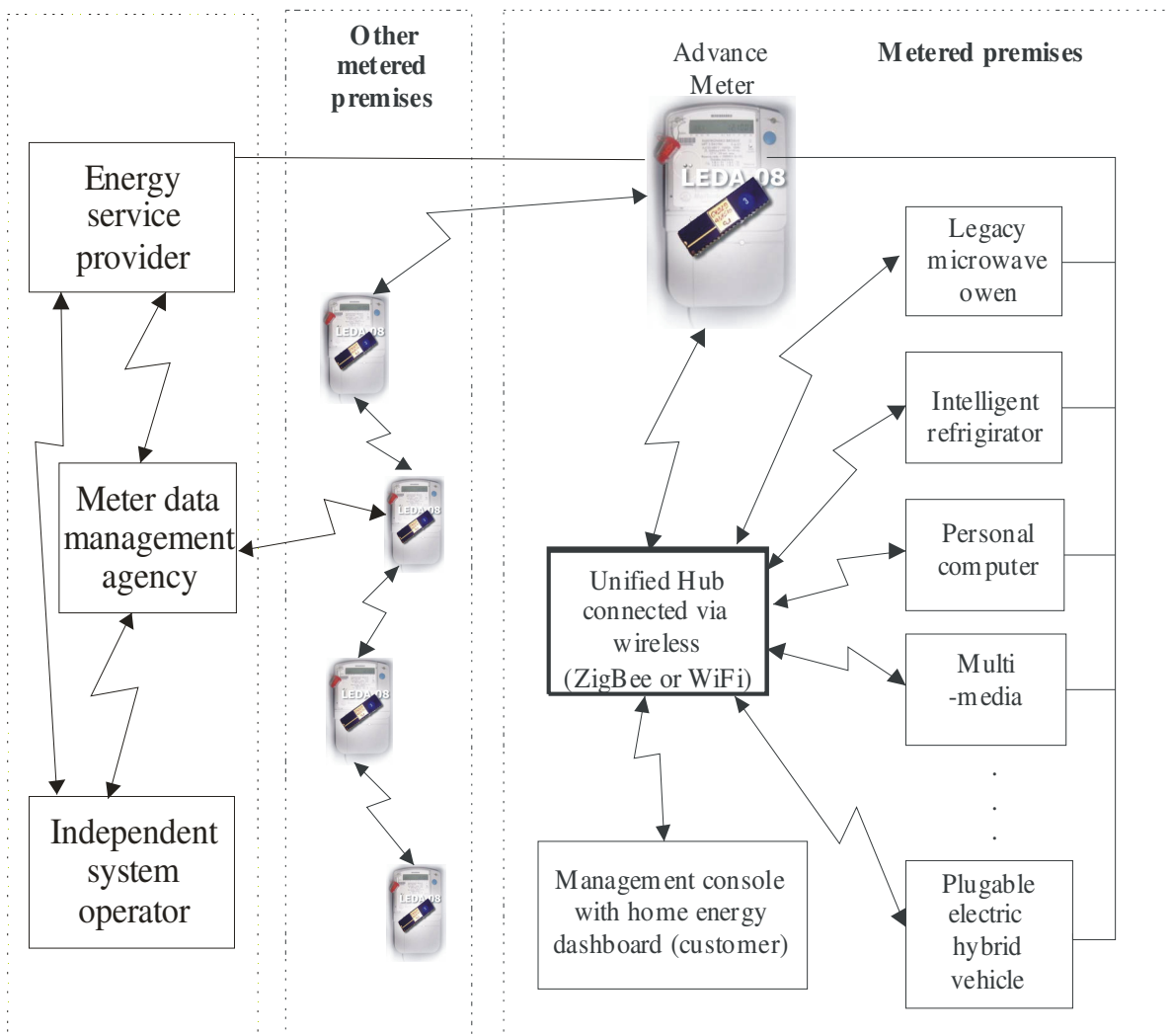
Fig. 3. The distribution network and the smart metering system seen as an ICT challenge for the future.

II. CRYPTOGRAPHY WITHIN THE GRID AND ITS IMPLEMENTATION IN POWER METERING DEVICE

Just as cellphones have become ubiquitous, mobile computing platforms, advanced meters may become the first ubiquitous, fixed (non-mobile) computing platforms. This could have a number of positive outcomes, such as the expansion of network access into currently unreachable areas. However, it also raises serious privacy concerns. The introduction of cellphones compromised the location privacy of customers, since the radio signals of cellphones can be tracked to determine the approximate locations of cellphone users. Similarly, advanced meters can potentially be used to determine not only whether a metered premise is occupied, but also how the occupants of the premise are currently behaving. This information could be correlated with location information to develop detailed profiles of those individuals, unless we control the dissemination of such information.

Another significant characteristic of advanced meters follows directly from the previous one. Massive meter deployments may lead to significant availability issues. If many meters attempt to transmit large quantities of data simultaneously, they may overload their communications infrastructure. This could interrupt service providers' income, if they are unable to collect billing data for significant periods of time. It could also lead to blackouts if load reduction signals are blocked or delayed.

While AMI could bring significant benefits, it is potentially subject to security violations such as tampering with the software in the meters, eavesdropping on its communication links, or abusing the copious amount of private data the new meters are able to collect. With anticipated deployments of millions of advanced meters, high costs for replacing meters, and greater dependence on AMI for the stability and financial integrity of the power grid, these threats must be taken seriously. In addition to securing market sensitive data from competitors, information systems for the power grid need to defend against malicious attacks that intend to harm the power grid as a whole. The more comprehensive an information system becomes, the greater the consequences of a successful attack and thus the need for security measures increases. In light of the last decade's developments in the world and the "war on terror" the need for securing the power grid against
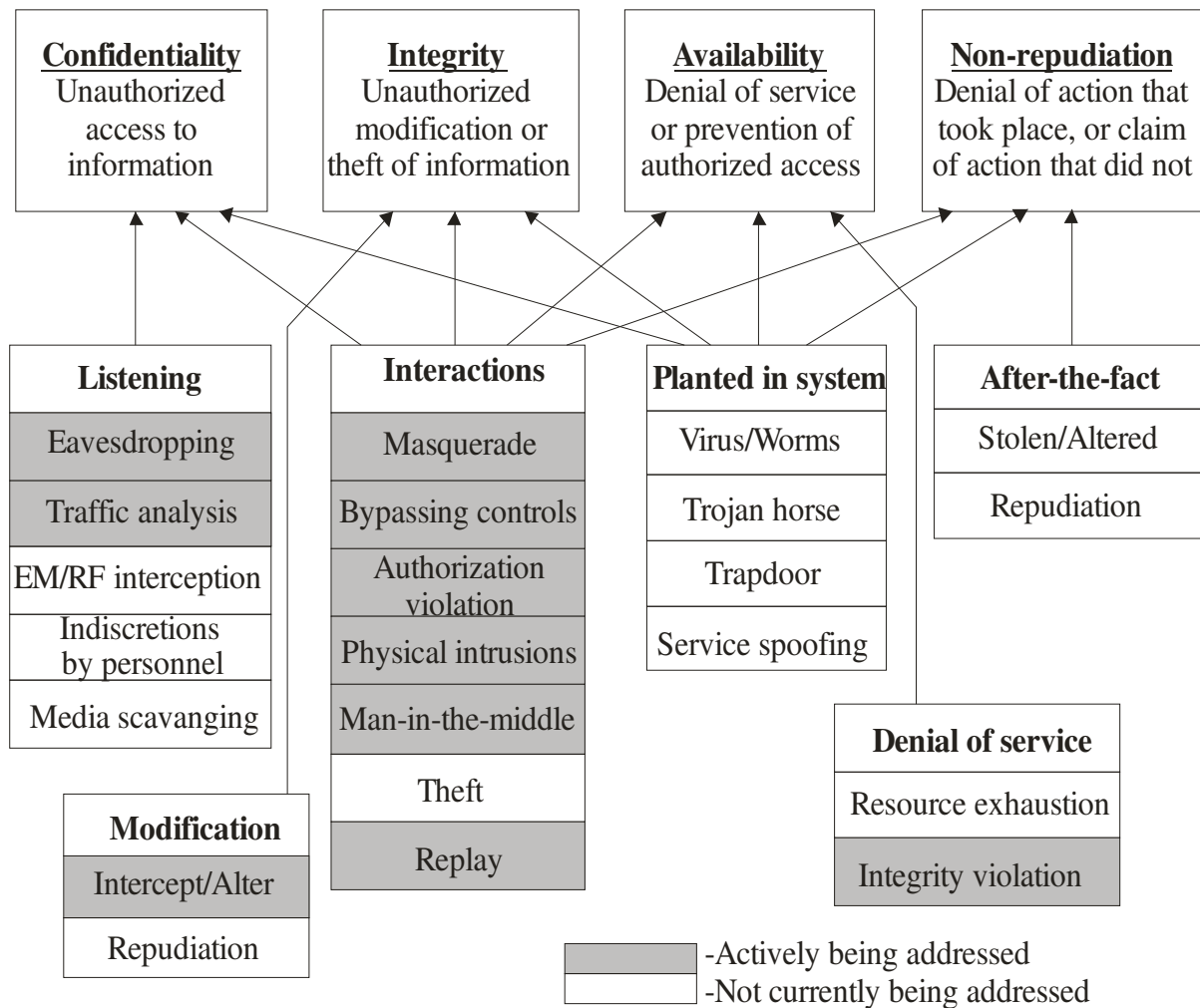
Confidentiality	Integrity	Availability	Non-repudiation
Unauthorized access to information	Unauthorized modification or theft of information	Denial of service or prevention of authorized access	Denial of action that took place, or claim of action that did not

Listening

Eavesdropping
Traffic analysis
EM/RF interception
Indiscretions by personnel
Media scavanging

Interactions

Masquerade
Bypassing controls
Authorization violation
Physical intrusions
Man-in-the-middle
Theft
Replay

Planted in system

Virus/Worms
Trojan horse
Trapdoor
Service spoofing

After-the-fact

Stolen/Altered
Repudiation

Modification

Intercept/Alter
Repudiation

Denial of service

Resource exhaustion
Integrity violation

- Actively being addressed
- Not currently being addressed

Fig. 4. Attacks defined by IEC TC57 WG15.

such attacks have been all around recognized [7].

A. The expected solution

In order to make a security system self-sufficient it needs to secure its own communication completely. Nothing is gained by adding security measures for the data plane while introducing new security weaknesses in the management plane, for example. Any security system needs to protect its own management communication by providing confidentiality, integrity and authentication in the same way as it provides it for the payload data.

We can divide the security problem into two main levels: the communication and the end-point security. After giving a short view to the security problem at the communication level we will properly address the end-point level and give some basic information on the design requirements of a cryptographic chip.

In the late 1990's the the International Electrotechnical Commission (IEC) Technical Council (TC) 57 Power Systems Management and Associated Information Exchange, which is responsible for developing international standards for power grid information systems, created a working group called WG15 to explore the security aspects of their protocols.

WG15 is an IEC TC57 working group with the title Power system control and associated communications - Data and communication security. Since its creation in 1997 it has tried to develop security mechanisms for the power grid information system. It has defined four main types of desired security properties:

- confidentiality,
- integrity,
- availability and
- non-repudiation

and explored how to provide safeguards against them. Fig. 4. depicts the types of attacks the group envisions and which types of attacks they actively try to address.

A standard named X.509 is being developed by the Public-Key Infrastructure working group (PK-IX) and was first proposed in 1988. It has gone through two major updates since then, one in 1993 and one in 2000 [8]. X.509 specifies standards for formats, certificates, certificate validation and a hierarchical composition of certificate authorities (CAs).

Certificates combine public keys with digital signatures and something that identifies them, e.g. an IP address. These certificates are sent from the server side to the client side (called an end-node in X.509 terminology) of a connection so

that the clients can authenticate the server by ascertaining that the signatures of the certificates are valid. Fig. 5 illustrates how public key cryptography can be used to accomplish this. If the signature is valid the client can conclude that the public key it received is the correct key for the server with the specified name and thus assume that the server is the only one that can decrypt messages encrypted with the public key.
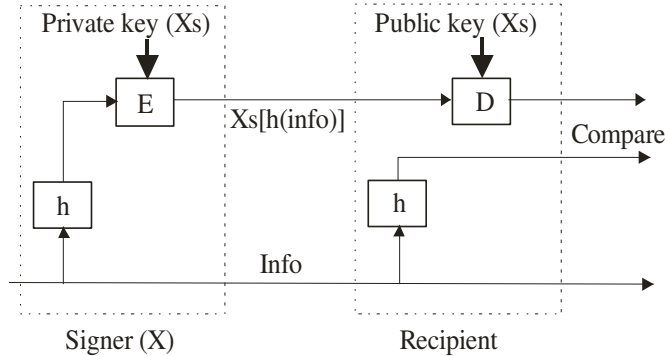

Fig. 5. Certificate signature validation (X.509).

There are two ways to sign a certificate, either it can be self-signed which means that the server signs his own certificate with its own key before sending it to the client. Self-signed certificates achieve little security when sent over-the-wire. The only thing a client can conclude from such a certificate is that whoever sent the certificate possesses the private key it was signed with. For self-signed certificates to provide any security they have to be loaded out of band from a trusted source [8].

The alternative way is to use trusted third parties CAs, to sign the certificate. By signing a certificate the CA endorses the server and says: If you trust me, you can trust that he is who he says he is. This assumes that the client already got the CA's public key installed and can use it to validate its signature.

A certificate may be revoked if it is discovered that its related private key has been compromised, or if the relationship (between an entity and a public key) embedded in the certificate is discovered to be incorrect or has changed. X.509 does this by checking if a certificate is valid through the use of a certificate revocation list (CRL) whose address is specified in the certificate.

A X.509 certificate roughly contains the following information:

- The public key being signed.
- A name, which can refer to a person, a computer or an organization.
- A validity period.
- Certificate Authority identification.
- The location (URL) of a revocation center.
- Name of the algorithm to use.
- The digital signature of the certificate produced by the CA's private key.

X.509 also defines an optional entity, called Registration Authority (RA), that complements the CAs by taking care of personal authentication, token distribution, revocation reporting, name assignment, key generation and archival of key pairs.

Public key infrastructures is build on public key cryptography, but only use it to achieve trust and to agree upon a faster and less resource greedy symmetrical session key for the real data transference. In this way the performance hit of using asymmetric algorithms can be partially mitigated.

Based on these and many other considerations systems are under developments that are to function as telecommunication system acting as an overlay over the grid [3,9]. It is our goal in the rest of this paragraph to define the basic functions and the proper location of the cryptographic integrated circuit that
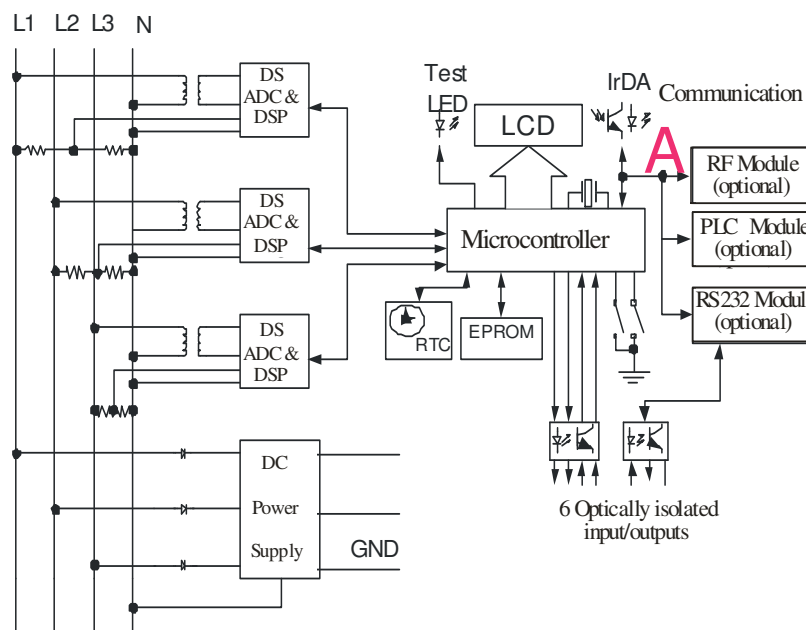

Fig. 6. Architecture of the advanced metering device produced by ATLAS Electronics.

would act as one of the actors in such a communication system at its end-points.

B. A cryptographic chip and its implementation

The cryptographic algorithms may be implemented both in software and hardware. Software solutions are cheaper and more flexible, while hardware implementations provide more speed and intrinsic security. In general, trade-off in cost and speed can be achieved by hardware software codesign.

A smart meter, however, is an example of a platform where the core port, i.e. the most computationally intensive part, is hardware-based, the hardware being custom designed. Accordingly, from now on we will consider the hardware implementation only.

When implementing public key cryptography the primary requirements are high speed arithmetic computation, small size and low power consumption, and resistance to SCAs. There are many sources in the literature describing hardware implementatons of the AES and RSA algorith.

In [10], for example, an optimized coding for the implementation of Rijndael (AES) algorithm for 128 bytes has been developed. The speed factor of the algorithm implementation has been targeted and a software code in VHDL that boasts of a throughput of 2.18 Gb/sec has been developed. The architectural innovations that have been incorporated in the coding include on the fly round key generation, which facilitates simultaneous execution of sub bytes, shift rows and mix columns and round key generation. A look up table called S-Box has been used to obtain the sub byte values instead of applying affine transformation every time to calculate sub byte values. This implementation was intended to be used in wireless security like military communication and mobile telephony where there is a greater emphasis on the speed of communication.

In [11,12] a review of techniques for implementation of the modular exponentiation operation in hardware is given. Techniques for exponentiation, modular multiplication, modular addition, and addition operations are discussed. In [13] an efficient way to build fast modular operation has been explored, using redundant digit sets with higher radices and making modifications to Montgomery's Algorithm in order to achieve deep pipelining at architecture level which improves the throughput and latency of the system. Alternative solutions were offered in [14].

On the other hand, the security of the implementation also needs to be considered. Namely, attacks on cryptographic algorithms are usually divided into mathematical (theoretical) and implementational (practical) attacks. The later are based on weaknesses in the implementation and can be passive and active [15]. The passive attacks are also called SCAs as they benefit from the side channel information that is achieved by measuring some physical quantity. The active attacks are more invasive as they are based on the introduction of faults that results in erroneous calculations leading to exposure of the secret key.

Serious research is under way searching for methods

hardening the designs against SCAs [16]. We intend to publish a separate overview of that subject. One should note, however, that information systems for the power grid have life expectancies of 25 years or more, and thus cause another serious technical challenge for this problem space. No one knows how much the computational power available to attackers will increase over such a long period of time, not to mention possible breakthroughs in ways to crack specific algorithms. This makes it very hard to design a static security system that with reasonable certainty can be trusted until the communication system someday is replaced.

III. CONCLUSION

A view to the future electricity distribution system and communications related to it were considered. Cryptography was advised as a must for protection of these systems against malicious users. Joining the efforts for best solution in the hardware implementation of cryptography for power metering devices, LEDA starts the design of a new chip to be placed in an existing power meter produced by ATLAS Electronics as shown in Fig. 6. The place wher the cryptographic chip is to be placed is marked by the letter A.

APPENDIX: BASICS OF PUBLIC KEY CRYPTOGRAPHY

It is already widely accepted that the success of the Information age depends on the ability to protect information as it flows around the world, and this relies on the power of cryptography. Encryption can be seen as providing the locks and the keys of the Information age [17]. The development of public key cryptography (PKC), particularly the RSA cipher [18] has given today's cryptographers a clear advantage in their continual power struggle against cryptanalysts. We intend to use PKC in our implementation and this is why we will here address the cryptography and the key exchange in some details.

Fig. 7. Basic flow of information within cryptography.

Until modern times, cryptography referred almost exclusively to encryption, the process of converting ordinary information (plaintext) into unintelligible gibberish (ie, ciphertext). (Fig. 7) Decryption is the reverse, moving from unintelligible ciphertext to plaintext. A cipher (or cypher) is a pair of algorithms which perform this encryption and the reversing decryption. The detailed operation of a cipher is controlled both by the algorithm and, in each instance, by a key. This is a secret parameter (ideally, known only to the communicants) for a specific message exchange context. Keys are important, as ciphers without variable keys are trivially breakable and therefore less than useful for most purposes. Historically, ciphers were often used directly for encryption or decryption, without additional procedures such as au-

thentication or integrity checks. If the same key is used for both encryption and decryption one speaks on symmetric keys.

In modern computer encryption and decryption procedures standardization was introduced meanning the complete procedure of encypherment was standardized leaving the key to be known to the communicating part as the only protection against eavesdropers. A standard that was mostly used is DES (Data encryption Standard) and his later version AES (Advanced decryption standard) introduced in the early seventies but still in use. It imposes, however, the problem of key distribution having in mind that many messages may be intended to be delivered to recipients all over the world. The problem was solved by using assymetric key pairs, a public and a privat key, in a procedure that is known as RSA, the name comming from the first laters of the family names of the authors.

While the symmetric key encription is performed by some algorithm of distorting the plaintext that produces different results wehen different keys are used, the RSA uses more complicated procedure enabling generation of cyphertext that is controlled by one side of the communication channel only. Becose of the importance of the subjec we will try here to express the essence of the procedure.

Since we use computer interpretaion of the text we may express the whole idea by numbers. Suppose the secret message to be transmitted is M. Two numbers are published by the receipient: e and N. N is suposed to be a very large number obtained by multiplication of two prime numbers: p and q, i.e. $N=p \cdot q$. p and q are kept secret by the receipient. e is referred to as the public key exponent. It is reqired e to be coprime with $\varphi=(p\text{-}1) \cdot (q\text{-}1)$ meanning that they share no factors other than 1. Now, the sender is creating the cyphertext i.e. he or she is calculating

$$C = M^e \big|_{\text{mod } N} \qquad (1)$$

For instance, if p=11, q=13, we get N=143 and φ=120. p, q, and φ are not known to the sender. For M=7, if e=7 one gets C=6. C is transmitted to the receipient. Note the importance of the modulo function. It is an one-way function that needs incomparably much more time to be inverted then to be calculated. For a very large N the problem of inversion is not tractable in a conceivable time.

Now the recipient performs the following calculations. First, one has to solve the equation

$$e \cdot d \big|_{\text{mod } \varphi} = 1 \qquad (2)$$

for d. In our example that is d=103. In general case this equation is solved by the so called Euclid's algorithm hence the complexity and time needed for performing the calculations. Finally, to decript the message one has to compute

$$\widehat{M} = C^d \big|_{\text{mod } N} \qquad (3)$$

which is the secret message: $M=(6^{103} \text{ mod } 143)=7$.

In case of a long message one brakes the original binary code into blocks, say 128 bit or more, and implements the above procedure to the blocks separately.

Instead of exponential the so called eliptic functions are used nowadays with much success.

It is conceivable now that the role of the recepient is the utilty company's computer that randomly produces public keys (e and N) using a very large pool of previously stored very large prime numbers (p and q). The public key is expected to be communicated to the metering device that will encript the information to be sent back.

If the private key is used to encrypt the message, every node with the public key can decrypt it, which means the message is not confidential, but since only the private key could have encrypted the message in the first place, the origin of the message can be authenticated. This is often called electronic signatures.

REFERENCES

[1] Hatziargiriou, N., "Microgrids, the key to unlock distributed energy resources", IEEE Power and Energy Magazine, Vol. 6, No. 3, May/June 2008, pp. 26-29.

[2] Kroposki, B., et all., "Making microgrids work", IEEE Power and Energy Magazine, Vol. 6, No. 3, May/June 2008, pp. 41-53.

[3] http://seclab.uiuc.edu/web/critical-infrastructur e/attested-metering.html

[4] Valocchi, M., Schurr, A., Juliano, J. and Nelson, E. "Plugging in the consumer, Innovating utility business models for the future", IBM Institute for Business Value, Somers, NY 10589, U.S.A., 2007. http://www-935.ibm.com/   services/us/gbs/bus/pdf/ibv_g510-7872-00_ plugging_in.pdf

[5] Jovanović, B., et all., "A new testing setup for integrated power meter", Proc. of the LI conf. of ETRAN, Herceg Novi, June 2007, Proc. on CD, EL2.5, R65.

[6] -, "IMPEG - An Integrated Power Meter IC", http://leda.elfak.ni.ac.yu

[7] Cleveland, F., "IEC TC57 security standards for the power systems information infrastructure beyond simple encryption". June 2007. IEC TC57 WG15 Security Standards White Paper ver. 11. http://xanthus-consulting.com/pages/publications.htm

[8] ITU Telecommunication Standardization Sector (ITI-T). ITU-T Recommendation X.509, July 2005, URL:http://www.itu.int/ rec/T-REC-X.509-200508-I/en

[9] Solum, E., "Achieving over-the-wire configurable confidentiality, integrity, authentication and availability in gridstat's status dissemination", M.S. Thesis, Washington State University, December 2007.

[10] Umamaheswari, G., and Shanmugam, A.," Efficient VLSI implementation of the block cipher Rijndael algorithm", Academic Open Internet Journal, Volume 12, 2004, http://www.acadjournal.com/2004/V12/Part5/p1/

[11] Kaya Koç, Ç., "RSA Hardware Implementation", RSA Data Security, Inc., Version 1.0, August 1995, http://security.ece.orst.edu/ koc/ ece575/rsalabs/tr-801.ps

[12] Kaya Koç, Ç.,, "High-Speed RSA Implementation". Technical Report TR 201, RSA Laboratories, November 1994. ftp://ftp.rsasecurity.com/pub/pdfs/tr201.pdf

[13] Shantilal, A. C., "A Faster Hardware Implementation of RSA Algorithm", Oregon State University, Corvallis, Oregon 97331 -USA, http://islab.oregonstate.edu/koc/ece679/project/ 2002/ajay.pdf

[14] Ziya Alkar, A., and Sönmez, R., "A hardware version of the RSA using the Montgomery's algorithm with systolic arrays", Integration, the VLSI Journal, Vol. 38, No. 2, Dec. 2004, pp. 299-307.

[15] Batina, L., et all., "Side channel attacks and fault attacks on cryptographic algorithms", Revue HF Tijdschrift, No. 4, 2004, pp. 36-45.

[16] Tiri, K., and Verbauwhede, I., "A VLSI design flow for secure side-channel attack resistant ICs," Proc. Design Automation and Test Conf. in Europe (DATE 2005), pp. 58-63, March 2005.

[17] Singh, S., "The code book", Fourth Estate (HarperColins Publishers), London, 1999.

[18] Konheim, A. G., "Computer security and cryptography", Wiley, Hoboken, N.J., 2007.

Statistical Timing Analysis of Asynchronous Circuits Using Logic Simulator

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Abstract—**The lack of methods and tools for performance estimations in asynchronous circuits is one of the main reasons why this design methodology, beside its advantages, is still unpopular among designers. Using a logic simulator it is possible to efficiently estimate all worst-case path delays in one asynchronous circuit, which can be crucial for overcoming this problem. This paper describes a method for statistical estimation of topological delays in asynchronous circuits, based on the application of a VHDL simulator. The method is verified on a set of chosen asynchronous circuits and in compare with other similar methods shows higher efficiency.**

Index Terms— **Asynchronous logic circuits, Logic simulator, Timing analysis.**

I. INTRODUCTION

ASYNCHRONOUS integrated circuits design style is the one that designers rather avoid, beside its unquestionable advantages. Asynchronous circuits don't have the clock signal, and the problems related to clock routing and distribution, such as the clock skew are avoided. The absence of the clock lines gives a significant size reduction for the integrated circuit. These circuits are characterized with a good modularity, easier technology migration and down scaling. The energy is consumed only while the useful work is done. The absence of the clock signal also significantly contributes to the reduction of the power consumption. These circuits have less EMI levels (and though the decreased emanation from the chip, which make the side-channel attacks easier), and are more resistant to noise. All those advantages are very important, especially while designing mobile systems where the battery size and its duration are the key factors [1].

Nevertheless, the absence of the clock signal means that the events in the asynchronous circuits cannot be accurately predicted, as it can be with the synchronous circuit, which is the mail reason for their poor design tools support. Also, synchronous circuits have a larger commercial practice [2].

All these issues give a weak motivation for the usage of this design style.

One of the problems related to the asynchronous circuit design technique that is still unsolved is the estimation of their performances. In other words, it is necessary to determine the delays of all paths in one asynchronous circuit. This estimation, performed in the earliest design stages, would significantly contribute to early detection of the bad design solutions, and would at the same time be used as a tool for the early estimation of the operation speed for the new designed circuit. More accurate delays could be determined in the final design steps, after the circuit layout synthesis. Though, if the obtained circuit operating speed is not satisfactory after all these steps, or a particular timing problem occurred, the circuit has to be redesigned, and the design brought back to the beginning. At the end, one can come to a conclusion that the performance estimation is the best to be performed in the early design stages, that is, right after the first circuit description and the simulation [3].

The simulation is the simplest way to determine a delay in a circuit. But, it is very inefficient to simulate large circuit at the transistor level of abstraction. Logic simulators use simplified gate models and significantly speed up this process. Using the logic simulations, it is possible to verify the logic function as well as the behavior of the circuit in the observed time period. Nevertheless, the delays obtained in this way depend on the applied combination of the input vector. In order to determine the largest and the smallest delays for a circuit, it has to be simulated for all possible 2^n input vector combinations, where n represents the number of circuit inputs. For the circuits with a large number of inputs this approach is also inefficient. At the other hand, since the logic simulator is used for the first design stages, implementing the method for worst-case delay estimation into the standard logic simulator, would ensure the early detection of the incorrect design solutions.

The second aspect that strongly affects the obtained integrated circuit yield is the tolerance of the technology. Even with the perfectly designed circuit, it could often happen that the use of more tolerant processes, gives many circuit that do not satisfy the required timings. In other words, we produce a circuit whose response is outside the acceptable limits. Parameters of the particular electronic circuit have the statistical distribution within a particular interval. Logic simulator which is enhanced with the procedures for worst-

case delay estimation, is capable to simulate these phenomena, in order to achieve more accurate estimation results, used in final yield estimation.

To achieve more accurate delay estimation results, another aspect must be taken into account, and that is the circuit implementation. The fanout value of each gate in the circuit netlist could be very important, but is often a neglected factor in the logic behavior and timing analysis. This fact brings one to a conclusion that this factor must be taken into account while implementing the method for a digital circuit path delay estimation.

In this paper we will try to demonstrate the application of the standard logic simulator in the worst-case delay estimation for all paths of the asynchronous circuit. The statistical delay estimation method that is suggested in this paper takes into account both the tolerances of the technology and the circuit implementation, while using a very accurate models of the gates' timing behavior. The advantages of this method are its simplicity, efficiency and the ability to be implemented it into any standard logic simulator. The following paragraphs will give the description of the method, its implementation into a VHDL simulator, and the procedures for statistical processing of the obtained results using the Matlab program.

II. ASYNCHRONOUS CIRCUIT DELAY ESTIMATION USING A LOGIC SIMULATOR

In order to enable timing analysis using a standard logic simulator, it is necessary that signal and gate descriptions carry the information about delays, while the signal logic values become irrelevant in this case. Signals should be described with a specific attributes which define events and delays. Signals described in this way activate processes inside the gates and change the current values of the signal attributes. In order to achieve the large speed of such an analysis, the simultaneous propagation of all possible input vector combinations through the circuit is assumed. Nevertheless, it does not mean that the circuit has to be simulated for every possible input vector combination. Instead of it, with one analysis run all possible input vector combinations are analyzed for each gate in the circuit and only those considered as worst-cases sent further through the circuit until the primary outputs of the entire circuit are reached. The delay values are accumulated along the paths in the circuit starting from the primary inputs, and ending at the primary outputs, or some other point inside the analyzed circuit. At the end of this, very fast process, the largest and the smallest delay values for the rising and the falling edges of all output signals are available.

For each signal S in the circuit, four delay types are estimated::

  --d1mn(S) – the shortest path delay for a rising edge at S,

  --d0mn(S) – the shortest path delay for a falling edge at S,

  -- d1mx(S) – the longest path delay for a rising edge at S, and

  -- d0mx(S) – the longest path delay for a falling edge at S.

In order to enable simultaneous propagation of all possible input vector combinations, and to enable the calculation of all mentioned delay values, signals that connect gates inside the circuit must carry two types of information. They are represented in a form of two types of attributes: attributes that carry the information about signal events, which initiate the calculation processes inside the gates, and the attributes that contain the information about all listed delay types.

Processes inside the gates caa process signals described in this way, and it requires two-modes gate models, that is: activation-propagation mode and the delay calculation mode. Also, in order to enable the calculation of all delay types, the description of a gate model must contain two processes: one for the calculation of the maximal delay for the rising and falling signal edges, and one for the calculation of the minimal delay for the rising and falling signal edges. The activation-propagation mode of the gate model in each of these processes is sensitive to any change of the attribute for initiation of the delay calculation. When this mode is activated, an output signal is given new value of the delay attribute, taking into account the values of the delay attributes for all gate input signals, and the particular delay value of the observed gate. When this value is updated, the initiating attribute of the gate output signal is also changed in order to initiate the delay calculations in the gates that topologically follow.

The basic principle of the delay accumulation process is described in figure 1. The figure illustrates the calculation of the maximal delays along all paths of one tree-input C element. In this case, both rising and falling edges are applied at all circuit inputs. Inside each gate, new delay values for rising and falling edges are obtained. The delay estimation process ends when all these transitions reach the circuit primary outputs. In this case the delay analysis along all the paths in the circuit is possible only after the feedback line is broken. It makes sense to analyze the delays along the paths of the circuit in only one operating sequence.

Nevertheless, it could also be interesting to determine the maximal delay along the signal paths that go through the feedback line. In this way it is possible to analyze the timing behavior for more operating sequences of the circuit. The suggested delay estimation method could be extended to analyze such cases, if one applies the principle similar to one used for sequential circuit test vector generation [4]. It means that in order to analyze timing of the few operating sequences in a circuit, that circuit should be replicated and analyzed that many times. Figure 2 illustrates the application of such a principle for estimating the delay of the longest path for an asymmetrical C-element circuit. It is also necessary to break the feedback, as shown in the figure. From the
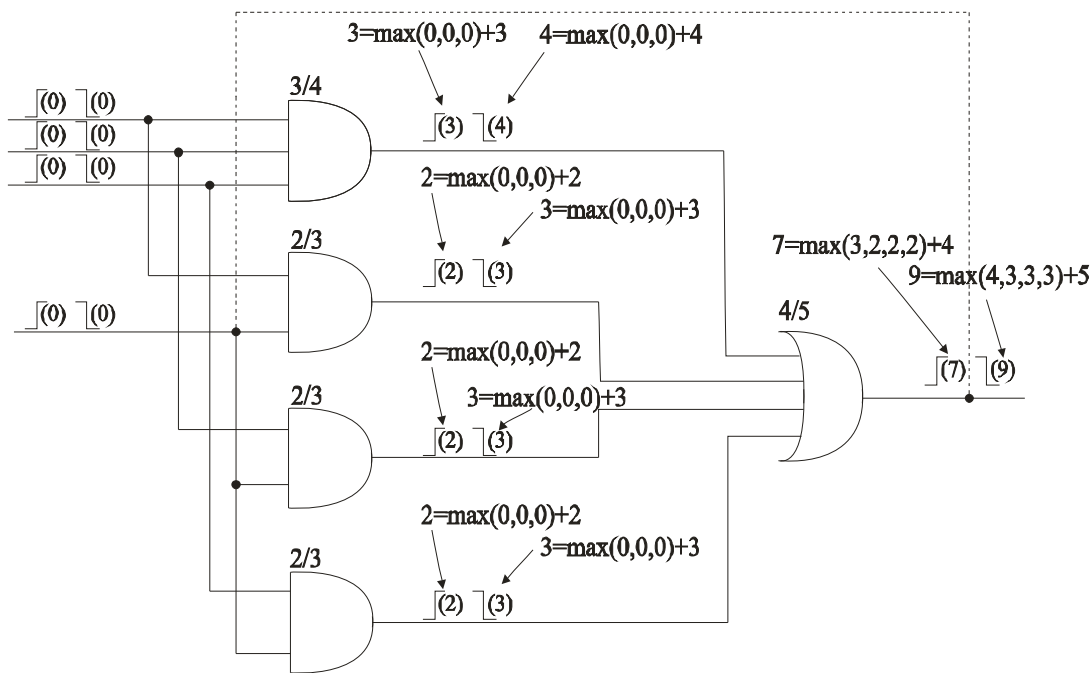
Fig. 1. The estimation of the maximal delay for a tree-input C element
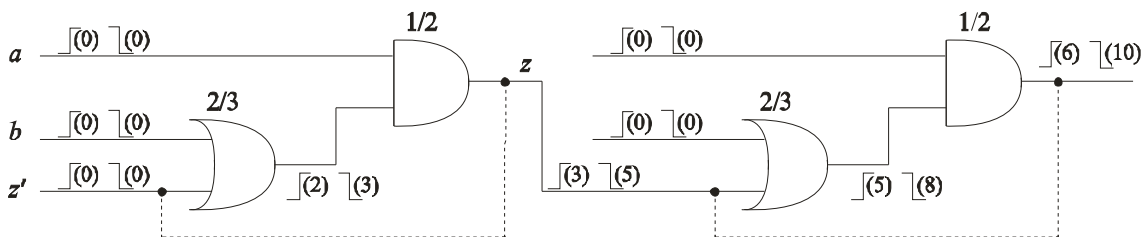

Fig. 2. Maximum delay estimation through the sequences

implementation point of view, the circuit netlist does not have to be rewritten few times. Instead, the results of the delay estimation processes should be applied to the input of the circuit that makes the feedback. After that, the circuit should be analyzed again, with a new initial delay parameter values.

Each gate is described with four types of delay. They are maximal delay of the rising edge through the gate, minimal delay of the rising edge through the gate, maximal delay of the falling edge through the gate and the minimal delay of the falling signal edge. Although these values are fixed for each gate, the delay assignment process in each gate is much more complex. Two factors determine the gate delay value. First, the real implementation of the circuit is taken into account and the particular gate position within the circuit netlist. It means that gate's fanout affects the gate delay and this dependence is expressed with a specific function. The second factor is related to the gate's initial delay value, and this value is fixed. But, since our intention is the statistical delay analysis and the estimation of the process tolerances influence, it is necessary to randomly generate the delay value, which is defined with its mean and deviation according to the given delay distribution. The mean represents the fixed

chosen, and in our case is set to 3% value. The Gaussian delay distribution function is applied. Whenever the delay calculation process is initiated inside a gate, a special function generates the random value [3].

Statistically satisfying estimation results can be obtained after few hundred analyses. This fact should not intimidate since these analysis require very little time. The exact number of simulations is determined with a required result precision. The circuit also has to be described at the structural level. At the beginning of the analysis, both rising and falling edges are simultaneously applied to all circuit inputs. All these events at the circuit inputs initiate the delay calculation processes in gates from the first topological level of the circuit. When these processes terminate, the delay attribute values of the gates' output signals can be updated, and the activation-propagation attribute values change in order to enable the delay calculation processes in the gates from the second topological level. This wave of calculation is moving from the primary inputs until the primary outputs are reached. The analysis then terminates, and it gives as a result, all delay attributes for all output signals in the circuit.

III. VHDL IMPLEMENTATION

As already mentioned, suggested concept is implemented in VHDL environment and analyses are done using standard VHDL simulator. The best way to compute numerous results obtained through the statistical analyzes is automatically, so for that purpose Matlab software package is used. This software contains integrated procedures for mean value and deviation calculation under the set of numerous samples, as well as the tools for drawing histograms for circuits with small number of outputs.

VHDL models of all gates and simple asynchronous elements are kept in a particularly developed library. Figure 3 shows the implementation of a two-input C-element. This description contains a numerous calls of `gauss_rng` function. This function, for a given mean value and deviation, randomly generates numbers with Gaussian distribution. In order to verify this function, a test environment is built under which this function was executed 600 times, with the adequate parameters sets. The results are processed using Matlab and the corresponding histogram is obtained, and given in figure 4, showing the excellent results.

```
p1: process (in1.d0mn, in1.d1mn, in1.arr0mn, in1.arr1mn,
             in2.d0mn, in2.d1mn, in2.arr0mn, in2.arr1mn)
        variable r,p: real;
        variable multipl : real;
begin
        multipl := real(ifo_izl);
        f<=fanout_func(multipl)
        r:= ((f*1.0) + (0.03*(gauss_rng)));
        p:= ((f*0.9 + (0.03*(gauss_rng)));
        if (in1.arr0mn and in2.arr0mn ) then
                    out1.d0mn  <= min(in1.d0mn, in2.d0mn) + r;
                    out1.arr0mn <= true;
        end if;
        if (in1.arr1mn and in2.arr1mn) then
                    out1.d1mn  <= min(in1.d1mn, in2.d1mn) + p;
                    out1.arr1mn<= true;
        end if;
end process p1;
p2: process (in1.d0mx, in1.d1mx, in1.arr0mx, in1.arr1mx,
             in2.d0mx, in2.d1mx, in2.arr0mx, in2.arr1mx)
        variable r,p: real;
        variable multipl : real;
begin
        multipl := real(ifo_izl);
        r:= (multipl*0.95 + (0.03*(gauss_rng)));
        p:= ((multipl*1.05) + (0.03*(gauss_rng)));
        if (in1.arr0mx and in2.arr0mx) then
                    out1.d0mx  <= max(in1.d0mx, in2.d0mx) + r;
                    out1.arr0mx <= true;
        end if;
        if (in1.arr1mx and in2.arr1mx) then
                    out1.d1mx  <= max(in1.d1mx, in2.d1mx) + p;
                    out1.arr1mx<= true;
        end if;
end process p2;
```

Fig. 3. VHDL implementation of the processes within the two-input C-element
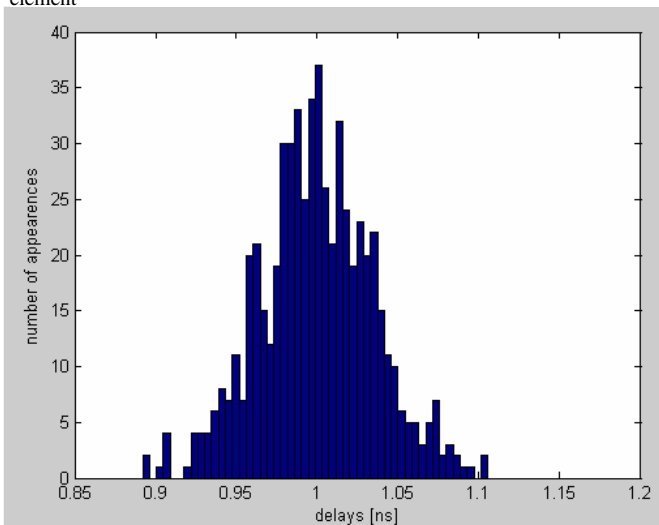
Fig. 4. Histogram of randomly generated values using a gauss_rng function

```
entity RSLatch is
        generic (ifo_izl_1: integer:= 1;
              ifo_izl_2: integer:= 1;
              tr_rq_mn : real := 1.0e-9;
              tf_rq_mn : real := 0.9e-9;
              tr_rq_mx : real := 1.05e-9;
              tf_rq_mx : real := 0.95e-9;
              tr_rnq_mn : real := 1.0e-9;
              tf_rnq_mn : real := 0.9e-9;
              tr_rnq_mx : real := 1.05e-9;
              tf_rnq_mx : real := 0.95e-9;
              tr_sq_mn : real := 1.0e-9;
              tf_sq_mn : real := 0.9e-9;
              tr_sq_mx : real := 1.05e-9;
              tf_sq_mx : real := 0.95e-9;
              tr_snq_mn : real := 1.0e-9;
              tf_snq_mn : real := 0.9e-9;
              tr_snq_mx : real := 1.05e-9;
              tf_snq_mx : real := 0.95e-9);
        port (q, nq : out SDA_std_logic := (0.0, 0.0, false, false, 0.0, 0.0,
        false, false);
              r, s : in SDA_std_logic := (0.0, 0.0, false, false, 0.0, 0.0,
        false, false));
end RSLatch;
architecture only of RSLatch is
begin
        p1: process (r.d0mx, r.d1mx, r.arr0mx, r.arr1mx, s.d0mx, s.d1mx,
        s.arr0mx, s.arr1mx)
                variable i, j ,k, l, m, n, o, p : real;
                variable multipl1, mulitipl2 : real;
        begin
                multipl1 := real(ifo_izl1);
                multipl2 := real(ifo_izl2);
                f1<=fanout_func(multipl1);
                f2<=fanout_func(multipl2);

                i:= (f1* tr_rq_mx + (0.03*(gauss_rng)));
                j:= (f1* tf_sq_mx + (0.03*(gauss_rng)));
                k:= (f2* tf_rnq_mx + (0.03*(gauss_rng)));
                l:= (f2* tr_snq_mx + (0.03*(gauss_rng)));
                if (r.arr0mx and s.arr1mx) then
                        q.d1mx<=max(r.d0mx,s.d1mx)+max(i, j);
                        q.arr1mx <= true;
                        nq.d0mx<=max(r.d0mx,s.d1mx)+max(k, l);
                        nq.arr0mx <= true;
                end if;

                m:= (f1* tf_rq_mx + (0.03*(gauss_rng)));
                n:= (f1* tr_sq_mx + (0.03*(gauss_rng)));
                o:= (f2* tr_rnq_mx + (0.03*(gauss_rng)));
                p:= (f2* tf_snq_mx + (0.03*(gauss_rng)));
                if (r.arr1mx and s.arr0mx) then
                        q.d0mx<=max(r.d1mx,s.d0mx)+max(m, n);
                        q.arr0mx <= true;
                        nq.d1mx<=max(r.d1mx,s.d0mx)+max(o, p);
                        nq.arr1mx <= true;
                end if;
        end process;
end only;
```

Fig. 5.   VHDL implementation of the RS-latch circuit – process for determining maximal delay to the circuit output

Figure 5 shows the implementation of the RS-latch circuit. It is assumed that this circuit has two inputs – R and S along with two outputs – Q and NQ. The definition of generics stands at the very beginning of the description. Beside 16 parameters representing the minimal and maximal delays of four possible input – output combinations (R-Q, R-NQ, S-Q, S-NQ) and both possible transitions, the generics description also contains the parameter corresponding to the fanout value ifo_izl. This parameter is initially set to unit value. Inside the netlist description, and during the instantiation of the particular library element, a specially developed program gives the real value to this generic, according to the circuit structure and its topological position [5]. For this particular circuit, two fanout values are required, since the circuit has two outputs. The figure shows the process for determining maximal delays to both outputs. Similar process stands for determining minimal delays.

A unique testbench programs enable the multiple simulations (600) of the analyzed circuit, while writhing the estimation results for all delay types for each circuit outputs into a specific text file. Matlab program reads the corresponding columns in these files and calculates its mean and deviation value for each circuit output. The described results analysis is appropriate for the circuits with a large number of outputs. For the circuit with a small number of outputs, the results can be represented in the form of a histogram.

IV. RESULTS

For a verification of the proposed delay estimation method a set of typical asynchronous circuit is chosen. The problem that occurred here is that there are no asynchronous benchmark circuits, for verification, analysis and comparison of performances for different methods.

TABLE I
DELAY ESTIMATION RESULTS FOR AN ASYNCHRONOUS COUNTER

Output	Delay type	Topol. level	min/ max	fanout	statistics	
					mean	deviat.
1.	mnr	4	3.7ns	3.7ns	3.704	0.705
	mxr	4	3.9ns	3.9ns	3.898	0.071
	mnf	4	3.6ns	3.6ns	3.599	0.681
	mnf	4	3.8ns	3.8ns	3.799	0.687

Table 1 shows the logic simulator delay analysis results for one asynchronous binary counter containing four T-latch circuit. The first column in the table denotes the number of the output, the second column stands for the delay type of the particular circuit output, while the third shows the topological level for the obtained value of the particular delay type. Following two columns give the worst-case delay analysis results, when fanout value does not and then does affects the delay calculation processes, while the delay generation is not random. The last two columns give the statistical processing of the obtained simulation samples, that is, mean and the deviation value for the particular delay type.
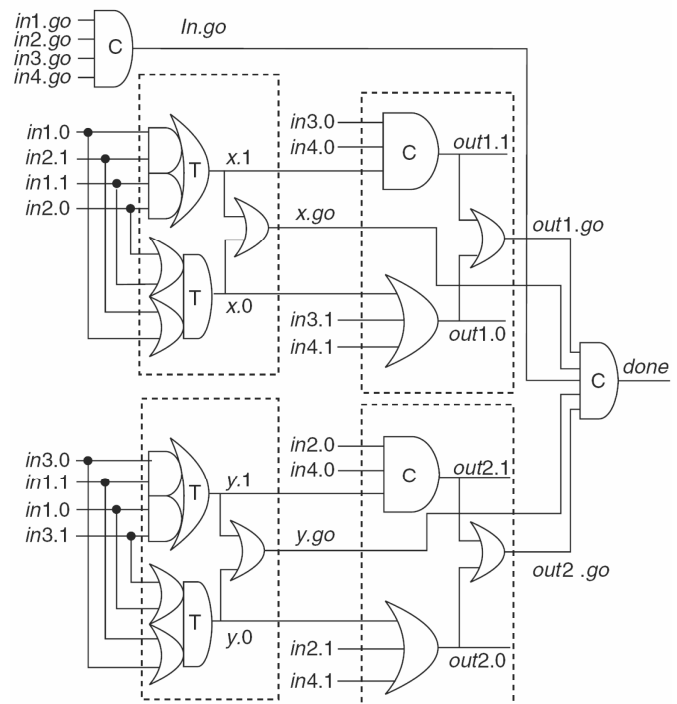

Fig. 6. Asynchronous encoder circuit

A more complex circuit of an asynchronous encoder is shown in figure 6, while the table 2 gives the analysis results for this circuit.

TABLE II
DELAY ESTIMATION RESULTS FOR AN ASYNCHRONOUS ENCODER

Output	Delay type	Topol. level	min/ max	fanout	statistics	
					mean	deviat.
1.	mnr	1	0.9ns	0.9ns	0.900	0.035
	mxr	1	0.95ns	0.95ns	0.954	0.036
	mnf	1	1.0ns	1ns	1.000	0.036
	mnf	1	1.05ns	1.05ns	1.051	0.035
2.	mnr	2	2.0ns	2ns	1.999	0.050
	mxr	2	2.1ns	2.1ns	2.101	0.050
	mnf	2	1.8ns	1.8ns	1.801	0.053
	mnf	2	1.9ns	1.9ns	1.905	0.049
3.	mnr	3	2.8ns	2.8ns	2.773	0.055
	mxr	4	4.0ns	4ns	4.000	0.072
	mnf	3	2.9ns	2.9ns	2.898	0.060
	mnf	4	4.0ns	4ns	4.000	0.072
4.	mnr	2	2.0ns	2ns	1.999	0.052
	mxr	3	3.05ns	3.05ns	3.051	0.060
	mnf	2	1.8ns	1.8ns	1.802	0.051
	mnf	3	2.95ns	2.95ns	2.954	0.064
5.	mnr	1	0.9ns	0.9ns	0.900	0.036
	mxr	2	2.0ns	2ns	2.002	0.053
	mnf	1	1.0ns	1ns	1.006	0.035
	mnf	2	2.0ns	2ns	2.002	0.049

Table 3 gives the simulation run times and the corresponding allocated memory for tree different asynchronous circuits: C-element, counter and encoder. The table gives the comparison for two delay analysis concepts: first is the analysis based on the concept described in this paper, while the second is based on the classical application of the standard logic simulations. The last column of this table shows how many simulations are required for a standard logic

simulator to simulate all possible input vector combinations. The table illustrates the significantly higher efficiency of the proposed method.

TABLE III
COMPARISON OF TWO DIFFERENT DELAY ANALYSIS APPROACHES

| Circuit | Timing analysis | | Logic simulation | | |
	memory allocation [kB]	CPU time [s]	memory allocation [кB]	CPU time [s]	number of simulations
C-elem	6.4	19.734	444	1	16
counter	7.7	20.277	375	2	2
encoder	28.5	92.583	480	436	1048576

V. CONCLUSION

A new concept of statistical worst-case delay estimation in asynchronous circuits is described in the paper. The method is implemented into a standard logic simulator.

Thanks to the specific gate modeling that includes the tolerances of the technology, the circuit specific structure, as well as different delay types that describe the gate's timing behavior, a high reliability of the obtained results is achieved. In compare with a classical Monte-Carlo analysis, the method shows higher efficiency from the allocated memory, and from the duration of the analysis points of view.

REFERENCES

[1] M. Lewis and L. Brackenbury, "CADRE: A Low-power Low-EMI DSP Architecture for Digital Mobile Phones," *VLSI Design*, vol. 3, issue 12, pp. 333-348, 2001.

[2] A. Davis and S. Novick, "An Introduction to Asynchronous Circuit Design," Technical Report UUCS-97-013, Computer Science Department, University of Utah, September 1997.

[3] M. Sokolovic, M. Zwolinski and V. Litovski, "New Concepts of Worst-case Delay Evaluation in Asynchronous VLSI SoC," Proc. 26th International Conference on Microelectronics, MIEL 2008, vol. 2, pp. 377-385, Niš, May 2008.

[4] K. T. Cheng and V. D. Agrawal, *Unified Methods for VLSI Simulation and Test Generation*, Kluwer Academic Publishers, 1989.

[5] M. Sokolović, V. Litovski and M. Zwolinski, "Fan-out Based Delay Estimation in Digital Circuits," *Proc. of the VI symposium on Industrial electronics*, INDEL 2006, pp. 101-104, Banja Luka, Nov. 2006.

Influence of Rotor Time Constant error on IFOC Control Structure

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Abstract—**This paper describes the influence of detuned value of induction motor rotor time constant parameter on overall performance of indirect field oriented control (IFOC) algorithm. The rotor time constant detuning sensitivity of IFOC drive is investigated in this paper. Presented computer simulation and experimental results show significant influence of parameter mismatch on IFOC structure, especially for high load values. Therefore, if significant rotor time constant drift is expected, an on-line estimation mechanism is required.**

Index Terms—**rotor time constant, induction motor, indirect field oriented control.**

I. INTRODUCTION

SPECIFIC advantages of induction motor over DC and DC-brushless motors lead to its progressive use in the speed and position controlled servomechanisms. In these motor drive applications, the shaft sensor is always present for the purposes of closing the space loops. Therefore, inherently more robust at low speeds, the indirect field orientation (IFO) controller is preferred choice for the drive with the position sensor [1]. However, since the feed forward slip calculation implies open-loop decoupling of the induction motor, the IFO controller is more sensitive to the plant parameters variation [2]. Hence, for the correct field orientation, the rotor time constant parameter (Tr*), used in the feed forward model, must fit the actual rotor time constant (Tr) of the motor. An inaccurate setting of that parameter results in an undesirable cross coupling and deterioration of the overall drive performance.

In this paper the initial rotor parameter is tuned based on equivalent machine model [3] and off –line tests like no load and load test. However, fluctuations of Tr are further caused by the thermal drift of the rotor resistance (Rr) and by the change of the motor inductances due to the nonlinearity of the main flux path magnetic circuit.

While the effects of the magnetic nonlinearity may be predicted and included into the IFOC feed-forward slip-calculator [4], the thermal drift presents a serious problem since the rotor temperature cannot be easily measured. For this reason, it is essential to investigate the influence of rotor time constant parameter mismatch on IFOC structure.

II. INDUCTION MOTOR MODEL WITH TWO STATE VARIABLES

Three phase induction motor has simple construction but unfortunate highly complex model and consequently complex control structure. The induction motor model can be build based on different state vectors. In this paper the model based on stator current and rotor flux state vectors is used. This model with stator current as state vector is suitable for most vector drives which already contain current regulated voltage source inverter –CRVSI.

Stator circuit voltage equilibrium equations, together with flux equations [5] make electrical part of induction motor model :

$$\vec{\mathbf{u}}_s = R_s \vec{\mathbf{i}}_s + \frac{d\vec{\psi}_s}{dt} + j\omega_{dq}\vec{\psi}_s$$
$$0 = R_r \vec{\mathbf{i}}_r + \frac{d\vec{\psi}_r}{dt} + j(\omega_{dq} - \omega_r)\vec{\psi}_r \tag{1}$$

$$\vec{\psi}_s = L_s \vec{i}_s + L_m \vec{i}_r$$
$$\vec{\psi}_r = L_m \vec{i}_s + L_r \vec{i}_r \tag{2}$$

where:

$$\vec{\mathbf{u}}_s = \begin{bmatrix} u_{ds} \\ u_{qs} \end{bmatrix}, \ \vec{\mathbf{i}}_s = \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} \ \text{i} \ \vec{\psi}_r = \begin{bmatrix} \Psi_{dr} \\ \Psi_{qr} \end{bmatrix}$$

are voltage, stator current and rotor flux vectors, but all ones in **dq** coordinate system, which rotates sinchronosly with field (speed ω_{dq}). Differential equation of rotor flux is:

$$\frac{d\vec{\psi}_r}{dt} = -R_r \vec{i}_r - j(\omega_{dq} - \omega_r)\vec{\psi}_r \tag{3}$$

Complex machine equations are:
- *Stator equation of model:*

$$T_\sigma \frac{d\vec{i}_s}{dt} + \vec{i}_s = -j\omega_{dq}T_\sigma\vec{i}_s + \frac{k_r}{R_\sigma T_r}(1 - j\omega_r T_r)\vec{\psi}_r + \frac{1}{R_\sigma}\vec{u}_s \qquad (4)$$

- *Rotor equation of model:*

$$T_r \frac{d\vec{\psi}_r}{dt} + \vec{\psi}_r = -j(\omega_{dq} - \omega_r)T_r\vec{\psi}_r + L_m\vec{i}_s \qquad (5)$$

where are:

$$T_\sigma = \frac{L_\sigma}{R_\sigma}, L_\sigma = L_s(1 - \frac{L_s L_r}{L_m^2}),$$
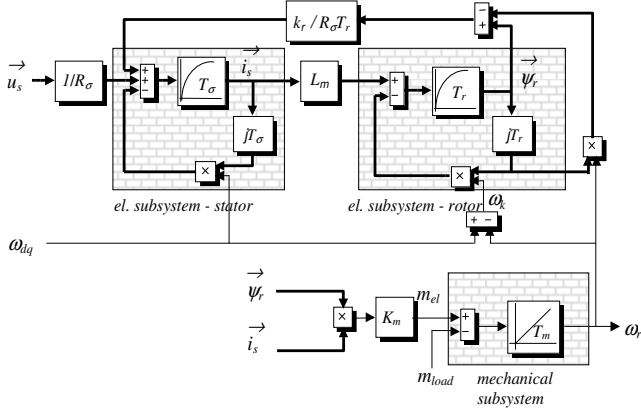
$$R_\sigma = R_s + R_r k_r^2, \quad k_r = \frac{L_m}{L_r}, T_r = \frac{L_r}{R_r}$$

Fig. 1. Model machine in complex domain with stator current and rotor flux vectors as state variables

The equation of mechanical subsystem is:

$$T_m \frac{d\omega_r}{dt} = \frac{3}{2} p \frac{L_m}{L_r}(\vec{\psi}_r \times \vec{i}_s) - m_{opt} \qquad (6)$$

where electromagnetic torque is shown as vector product of rotor flux and stator current. Block diagram of complex signals of this model is shown on fig 1.

III. INDIRECT ROTOR FLUX ESTIMATION MODEL

Efficiently driving of asynchronous motor can be done by adjusting frequency and voltage RMS or current RMS. Additionally, choosing right phase attitude of control stator value, it is possible to achieve same effects as they exist at direct current motor with independent excitation.

In order to have optimal vector control of asynchronous motor, it is necessary to control flux and electromagnetic torque independently [1]. Control contour for this variables can be separated by regulation amplitude of stator magnetize excitation force and its relative position in respect of rotor flux vector. Magnetizing excitation stator force can be controlled by current regulated voltage inverter (CRVSI). By elimination of stator voltage equations, electrical subsystem model is simplified and it consists of only one vector equation (5).

In the case of ideal current regulation, in motor is imposed current vector which amplitude and phase attitude are the same as reference. In this way, it is possible to exclude electrical subsystem from analysis. But, in order to have independent control, it is still necessary to know rotor flux position.

Rotor flux position is calculated by algorithm of indirect vector control. In this algorithm, position estimation is done in current model of rotor, which on behalf of stator current vector and mechanical rotor position simulates rotor occurrences.

In a case of ideal current regulated voltage inverter, it can be considered that measured and referenced component stator currents are identical. Therefore, referenced stator component can be used as input in rotor electrical subsystem.

By setting adequate referenced values to current regulated voltage inverter, it is possible to achieve desired complex vector input stator current on desired frequency excitation field (ω_{dq}).

As far as rotor frequency is known (it is provided by measure or estimation of that value), by control frequency of excitation field is practically controlled slip frequency ω_k.

The use of current regulated voltage inverter gives simplified machine model, still there is not provided independent flux and electromagnetic torque control. In that case, quadrature stator component change would induce rotor flux change, not only torque change. That torque change would not be linear with quadrature stator current increase.

Current regulated voltage inverter beside stator currents amplitude, control frequency of stator rotating filed ω_s. In a case of known electrical rotor frequency ω_r, it is obviously possible to control slip frequency.

In the event that rotor flux vector is set exactly on *d* axis, it makes flux and torque control independent (i_{qs} value does not influence on rotor flux). It means that if ψ_{qr} is equalized with zero, it gives [1]:

$$\omega_k = \frac{L_m i_{qs}}{T_r \psi_{dr}} \qquad (7)$$
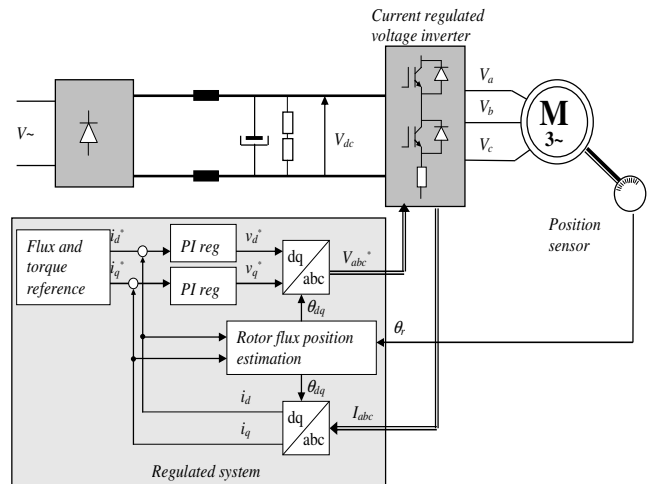
i.e. rotor q flux is zero (8).

Fig. 2. Schematic of vector controlled motor with current regulated voltage inverter

$$T_r \frac{d\psi_{qr}}{dt} + \psi_{qr} = 0 \qquad (8)$$

Therefore, rotor vector flux on **d** axis is:

$$T_r \frac{d\psi_{dr}}{dt} + \psi_{dr} = L_m i_{ds} \qquad (9)$$

In this way, it is possible to control amplitude rotor flux only by change of **d** component stator current, completely independent of **q** component.

Moreover, the expression for electromagnetic torque is simpler, for the same change of flux amplitude it is given linear torque change with change of stator **q** component [1]:

$$m_{el} = K_m \psi_{dr} i_{qs} \ , K_m = \frac{3}{2} p \frac{L_m}{L_r} \qquad (10)$$

In this way, command flux and torque contour are independent, therefore it is possible to have optimal control of asynchronous motor.
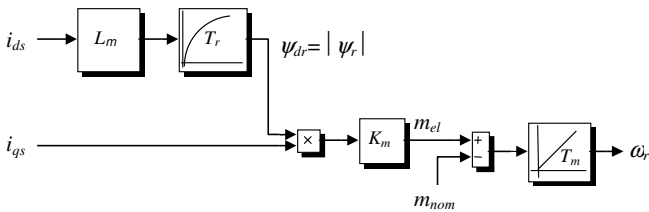
Fig. 3. Simplified model of asynchronous machine

IV. INFLUENCE OF ROTOR TIME CONSTANT ERROR ON IFOC CONTROL

One of the most important tasks of DSP is to calculate all relevant quantities from the model (Fig. 2) in a real time. If the calculations are done according to a real model and in a efficient time, orientation of rotor flux vector is correctly evaluated and independent motor flux and torque control is fulfilled.

Shown model use rotor electrical time constant T_r^* as a parameter, so the model is highly sensitive to its error. If the assumed value of the parameter T_r^* is not consistent with real value $T_r = L_r / R_r$, orientation of rotor flux vector is not correctly estimated. In that case, flux and torque control loops are not independent.

Based on mathematical model of vector controlled induction motor and with the drive simulation in *Matlab*, it could be seen how the potential source of error in T_r^* will affect IFOC drive. In a drive with position sensor, indirect determination of rotor flux vector is directly dependent on slip calculation. Direct component of flux vector in stationary state has a form [1]:

$$\psi_{dr} = L_m \cdot i_{ds} \qquad (11)$$

so the slip could be calculated as:

$$\omega_k = \frac{1}{T_r} \cdot \frac{i_{qs}}{i_{ds}} \qquad (12)$$

In Eq. (12) i_{qs} and i_{ds} are command input values for slip calculator.

In indirect vector control constant $k_{Tr} = 1/Tr$ is of interest, i.e. whole drive structure is dependent on accurate determination of parameter k_{Tr}.

Simulation with k_{Tr} parameter variation is considered on loaded motor with m=1.5[Nm]. Motor is started from zero speed and in a moment *t=4s* parameter k_{Tr} is increased for 20%, until moment *t=8s* when it is decreased for 20% regard to the accurate value. As could be seen from simulation results in Fig. 4, orientation of synchronous reference frame is lost with the change of parameter k_{Tr}. As an implication of that vector control is also lost which is occured with quadrature component in rotor flux vector ψ_{qr}.

With lose of vector control there is considerable change in stator current quadrature component, as an implication of changing parameter k_{Tr}. In the no-load case, change of parameter k_{Tr} will not affect motor flux and stator current quadrature component.
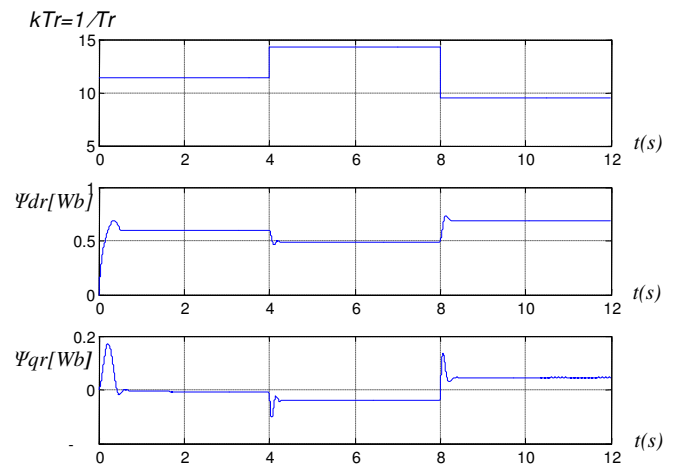
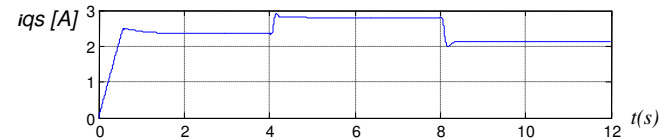Fig.4. Simulation results – loaded (m = 1.5 [Nm]) motor flux variation with the change of parameter kTr (±20%).

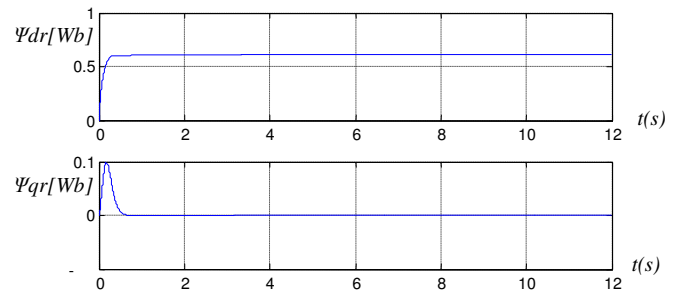Fig.5. Simulation results – loaded (m = 1.5 [Nm]) motor current i_qs variation with the variation of parameter kTr (±20%).

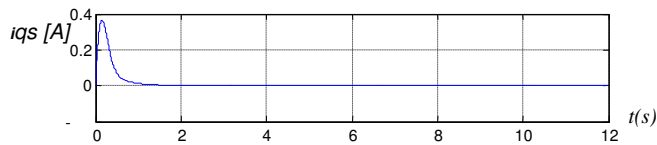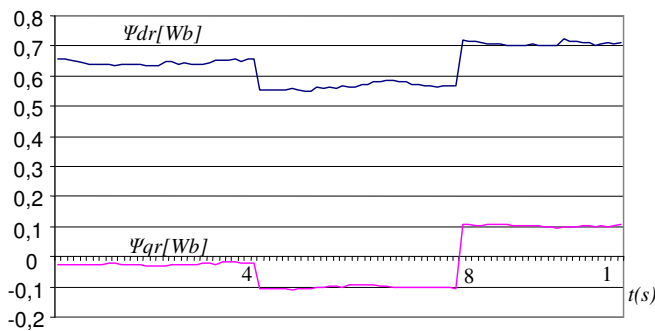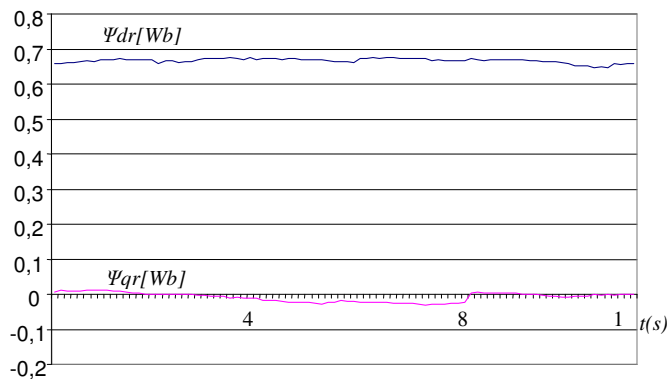Fig.6. Simulation results – no-loaded motor flux variation with the variation of parameter kTr (±20%).

Fig.7. Simulation results – no-loaded motor current iqs variation with the variation of parameter kTr (±20%).

V. Experimental verification

Experimental results are done with the motor whose data are used in mathematical model in *Matlab* simulation. With the Freescale DSP 56F8013 as a control unit, simulation results are practically confirmed. Experimental results are shown in Figs. 8 and 9.

Sl.8. Experimental results – loaded (m=1.5 [Nm]) motor flux variation with the variation of parameter kTr (±20%).

Sl.9. Experimental results – no-loaded motor flux variation with the variation of parameter kTr (±20%).

VI. Conclusion

This paper shows high sensibility of IFOC drive to incorrect value of rotor electrical time constant. Moreover, it is shown that sensibility is increased as a motor load is increased. So, rotor time constant must be tracked down during whole drive operation, since to magnetic field saturation level and also since to temperature change. According to unpredictable influence of other physical quantities, it is needed to incorporate on-line mechanism (during the drive operation) for rotor time constant identification.

REFERENCES

[1] V. Vučković, *Električni pogoni,* Beograd: Akademska misao, 2002.
[2] K.B. Nordin, D.W. Novotny, D.S. Zinger. The Influence of Motor Parameter Deviations in Feedforward Field Orientation Drive Systems. *IEEE Trans. on Ind. Appl.* July/August 1985; vol IA-21, No 4: 1009 - 1015.
[3] G. Rašković, *Određivanje zagrejanja i prevalnog momenta trofaznog asinhronog kaveznog motora*, Novi Sad: Fakultet teničkih nauka ,diplomski rad, 1989.
[4] F.M. Khater, et. al. Selection of Flux Level in Field Oriented Induction Machine Controllers with Consideration of Magnetic Saturation Effects. *IEEE Trans. on Ind. Appl.* March/April 1987; vol IA-23, No 2: 276 - 282.
[5] V. Vučković, *Opšta teorija električnih mašina*, Beograd: Nauka, 1992
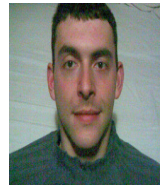
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Calibration of High Voltage Linear Voltmeter

M. Azlen, S. Milovančev, and V. Vujičić

Abstract—**In this paper, linear voltmeter for direct measuring on 20 kV voltage level is described. Its main feature is linearity, what is verified theoretically and experimentally.**

Index Terms—**harmonic measuring instrument, linearity, voltmeter, testing.**

I. INTRODUCTION

NOWDAYS, high voltage measurement is mainly made by high voltage measuring transformers which adapt measured voltage to measurement range of instrument, and after that by the instrument itself – with voltmeter. On very high voltages (over 110 kV), capacitive dividers are used. The key element is the voltage transformer. Recently, the high voltage resistor divider has appeared.

On low voltage side (0.4 kV), especially in electric energy meters, voltage resistor dividers are used for voltage measurement. Both these solutions, voltage resistor dividers and voltage measuring transformers, in addition to useful features being ground of application, they have some disadvantages:

    a) Voltage measuring transformer is nonlinear
    b) With voltage resistor divider there is no galvanic separation of the instrument from the measured voltage.

In the paper [1], it is putting forward as a measuring method of net voltage which is overcoming the both mentioned disadvantages: stochastic measuring method. It uses series resistor at the input and transformer without core (mutual inductance) so the measurement is completely linear and the galvanic separation of the input from the measuring instrument is accomplished.

The coreless transformer has a very feeble output signal, in other words, it has a low signal/noise ratio, however, in literature [2] it is demonstrated that the stochastic method can overcome this problem successfully and the noise is being firmly suppressed independently on probability distribution function. In addition, the applied measuring method eliminates the serious problem appearing with high voltage resistor divider – dependence of dividing factor on input voltage. The resistor is simply in function of series resistor here and there is no voltage dividing.

In the second chapter, the built linear voltmetar is described as it follows:

in *A*. the principle of functioning of linear voltmeter is described, and in *B*. the principle of functioning of Harmonic Measuring Instrument (HMI), which is explained in details in [3].

In Chapter 3, the problem of experimental testing of metrological properties of built linear high voltage voltmeter is described, as well as the testing itself.

In Chapter 4, the testing procedure is discussed briefly, and in 5. a short conclusion is given.
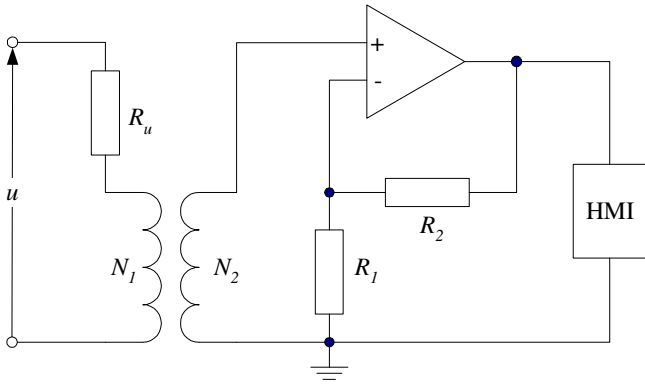
II. LINEAR VOLTMETER

A. Proposal of New Linear Voltmeter

The list of denotations:

U – measured input voltage,

R_u - series resistor,

u_2 - secondary winding voltage,

e_2 - induced electromotive force on secondary winding,

U_2 - RMS value of secondary voltage,

L_1, L_2, L_{12} - primary inductivity, secondary inductivity, mutual inductivity,

I - RMS value of primary current,
ω – angular frequency of fundamental harmonic,

E_1 - RMS value of electromotive force on primary winding,

E_2 - RMS value of electromotive force on secondary winding,

M – dimensionless constant,

u_{2i} - amplitude of ith harmonic on secondary,

U_i - amplitude of ith harmonic of input voltage u,

φ_{2i} - phase of ith harmonic on secondary,

φ_i - phase of ith harmonic of input voltage u,

Γ_{NA} - relative error (nonlinearity) of amplitude,

Γ_{NF} - relative error (nonlinearity) of phase.

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The proposed linear voltmeter is showed on Fig. 1.

(HMI – Harmonic Measuring Instrument)

Fig. 1. Scheme of new linear voltmeter.

The absence of core in this transformer, showed in this picture, allows the instrument to be linear and there is also galvanic separation from measuring circuit.

$\breve{U}_{2i}$ is i[th] harmonic of input voltage on amplifier in complex form and it is given with expression

$$\bar{U}_{2i} = \frac{ji\omega L_{12}}{R_u + ji\omega L_1} \cdot \bar{U}_i \qquad (1)$$

where $\breve{U}_i$ represents i[th] harmonic of phase-to-phase voltage in complex form.

It is supposed that the taken voltage value is U=600 V and the primary current is (current in primary winding) I=1 mA.

Because of absence of core the inductivities L_1 and L_2 are considerable small, and I=$\dfrac{U}{R_u} \Rightarrow R_u = 600\text{k}\Omega$.

Current in secondary winding because of amplifier coupling is tending to zero, so we have I_2 =0.

Suppose that $N_1 = N_2$ =2000 turns and the diameter of each winding is r=1cm.

Intending to get $U_2 = E_2$ we suppose that $L_1 \approx L_2$, $L_{12} \approx \sqrt{L_1 L_2} \approx L_1$, where L_1, L_2 i L_{12} are inductivities of primary and secondary windings and mutual inductivity.

In case of sine current the electromotive force is:

$$E_2 = \frac{\mu_0}{2} \cdot N_1 N_2 r \pi \omega I \qquad (2)$$

If the frequency f=50Hz, than the electromotive force is E_2 : $E_2 \approx 25 \cdot 10^{-3}$ V .

As mentioned $L_1 \approx L_2 \approx L_{12}$, it succeeds that:

$$\frac{E_2}{U} \approx \frac{E_1}{U} = \frac{\omega L_1}{\sqrt{R_u^2 + \omega^2 L_1^2}} \text{ , and} \qquad (3)$$

$$E_1 = \frac{\omega L_1}{\sqrt{R_u^2 + \omega^2 L_1^2}} \cdot U \approx E_2 \qquad (4)$$

Generally, in case of ith harmonic:

$$\bar{U}_{2i} = \frac{ji\omega L_{12}}{R_u + ji\omega L_1} \cdot \bar{U}_i \approx \frac{ji\omega L_1}{R_u + ji\omega L_1} \cdot \bar{U}_i \qquad (5)$$

where $\breve{U}_i$ and $\breve{U}_{2i}$ i[th] harmonics of input voltage and to it corresponding secondary voltage.

From expression (5) we get:

$$\frac{U}{E_2} \approx \frac{U}{E_1} \approx \frac{R_u}{\omega L_1} \approx M \approx 24000 \frac{\pi}{4} \qquad (6)$$

In case of sine voltage and fundamental frequency f=50Hz.

The electromotive force e_2 is considerable small and it should be augmented into voltage range of ±2.5V amplifying k times.

Basing on expression (6):

$$\bar{U}_{2i} = \frac{ji \dfrac{R_u}{M}}{R_u + ji \dfrac{R_u}{M}} \cdot \bar{U}_i = \frac{ji}{M + ji} \bar{U}_i \qquad (7)$$

Amplitude of ith harmonic on secondary is given by expression:

$$U_{2i} = \frac{i}{\sqrt{M^2 + i^2}} \cdot U_i \qquad (8)$$

Its phase is:

$$\varphi_{2i} = i \cdot \frac{\pi}{2} - \arctan \frac{i}{M} + \arg\left(\breve{U}_i\right) \qquad (9)$$

When $M \gg i_{max}$, including $i_{max} = 50$, the next expression is given by:

$$U_{2i} \approx \frac{i}{M} \cdot U_i \text{ , i} \qquad (10)$$

$$\varphi_{2i} \approx i \frac{\pi}{2} - \frac{i}{M} + \varphi_i \qquad (11)$$

Expressions (10) and (11) are showing fundamental linear relation between amplitude and phase of ith harmonics of voltage on secondary winding u represented in figure 1.

Expressions (10) and (11) are very suitable for calibration than they are linear, but there is a question of linearity limits?

The response is given by quadratic member in expansion of expressions (8) and (9). In utility (distribution) systems 50 harmonics are significant, $i_{max} = 50$.

As mentioned above, it is supposed

$$\frac{1}{\sqrt{M^2 + i^2}} \approx \frac{1}{M} \qquad (12)$$

for the amplitude and the phase angle

$$\tan \frac{i}{M} \approx \frac{i}{M} \qquad (13)$$

Expression can be showed as:

$$\frac{1}{M}\left(1 - \frac{1}{2} \cdot \frac{i^2}{M^2}\right) \approx \frac{1}{M} \qquad (14)$$

Relative error because of previous assumption gives nonlinearity:

$$\Gamma_{NA} = \frac{i^2}{2M^2} \le \frac{i_{max}^2}{2M^2} = 0.000\ 002\ 2 \quad (15)$$

Which is not bigger than 2,2 ppm.

Expression (13) can be represented as

$$\frac{i}{M} \cdot \left(1 + \frac{1}{3} \cdot \frac{i^2}{M^2}\right) \approx \frac{i}{M} \quad (16)$$

Relative error because of previous assumption gives nonlinearity:

$$\Gamma_{NF} = \frac{i^2}{3M^2} \le \frac{i_{max}^2}{3M^2} = 0.000\ 001\ 5 \quad (17)$$

which is not bigger than 1,5 ppm.

B. Integrated Instrument for Measurement of Harmonics

Integrated instrument for measurement of harmonics (HMI) is quoted in section *A*.

This paper gives its most important features. Its scheme is showed in the Fig. 2.
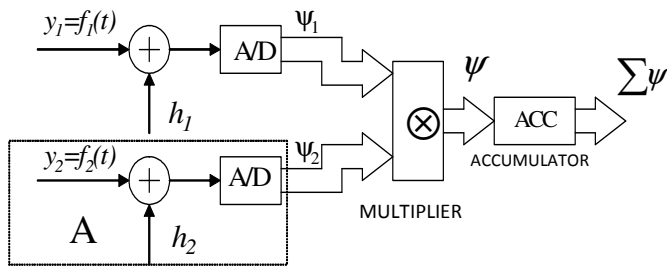
Fig. 2. Integrated instrument for measurement of harmonics.

In the realized instrument, block A is replaced by a memory block which contains samples of basic functions, for example $y_2 = f_2(t) = R \cos i\omega t$, and its output value is Ψ. After one period of fundamental frequency we get

$$\overline{\Psi} = \frac{R}{2} a_i \text{, where } a_i = \frac{2}{T} \int_0^T f_1(t) \cos i\omega t \, dt \text{, } (i = 0, 1, 2, ..., m).$$

If the memory unit contains $y_2 = f_2(t) = R \sin i\omega t$, than the output is $\overline{\Psi} = \frac{R}{2} b_i$ i $b_i = \frac{2}{T} \int_0^T f_1(t) \sin i\omega t \, dt$.

In our HMI, resolution of A/D converter is 6 bits. Resolution of basic functions is 8 bits, range R (range of converter) is $\pm 2,5V$, the frequency is 250kHz and the frequency of measured signal is f=50Hz.

It should be noticed that:

$$U_i = \sqrt{a_i^2 + b_i^2} \text{, and} \quad (18)$$

$$\varphi_i = \arctan\frac{b_i}{a_i} \quad (19)$$

HMI measures a_{im} and b_{im}. Voltage u_2 (secondary voltage) is amplified k times, so:

$$U_{2i} = \frac{\sqrt{a_{im}^2 + b_{im}^2}}{k} = \frac{i}{M} \cdot U_i \quad (20)$$

$$U_i = \frac{M}{i \cdot k} \sqrt{a_{im}^2 + b_{im}^2} = \frac{M}{i \cdot k} \cdot U_{2i} \quad (21)$$

And the phase is :

$$\varphi_i = \arctan\frac{b_{im}}{a_{im}} - i \cdot \left(\frac{\pi}{2} - \frac{1}{M}\right) \quad (22)$$

On the other hand RMS value of measured voltage is given by:

$$U = k_p \cdot \sqrt{\frac{U_{1m}^2}{1^2} + \frac{U_{2m}^2}{2^2} + ... + \frac{U_{nm}^2}{n^2}} \quad (23)$$

HMI instrument measures voltage derivative and shows that i^{th} harmonic is augmented i times, as the expression (21) shows, each harmonic should be divided by i.

That means, taking the result into consideration, that the upper limit of absolute error of each measured harmonic is constant and independent on the order of harmonic wave form [3] (measurement error of ith harmonic is i times smaller), that the higher harmonics can be measured more precisely.

III. PROBLEMS OF TESTING

According to the fact that The Faculty of Technical Sciences do not have high voltage laboratory, testing of the high voltage voltmeter popped up as a serious problem. The first problem is solved by getting high voltage from transformer oil testing device "RR Zavodi Niš - Munja ".

The second problem was the accurate measurement of high voltage. For this purpose, high voltage electrostatic voltmeter "S 196" is used. It has class 1, measures RMS value and has quadratic scale. The measurement reach is 30 kV, and has three ranges 7,5kV; 15kV; 30kV. The authors opted for range of 15kV, namely 11,5kV in regard to earth.

The series resistor is assembled from carbon layer resistors 470kΩ, so the current which flows through primary winding for full range of 11,5kV makes about 1mA.

Voltage amplifier with amplification factor equal to 51 is put on the output of secondary, so the voltage on that instrument, for full range, is 1,085V RMS, the value of amplitude on the input of instrument is 1,085·1,14≈1,53V accordingly.

We noticed that resistors closer to "higher" end are warmer, that leads to conclusion that they have greater resistance. It is clear that carbon layer resistors cannot be used as high voltage dividers. When the measurement has held on longer, especially, with higher values (about 10kV), the reading was instable and that is the reason not to use carbon layer resistors as series resistor. The only solution is to put new, stable, high voltage measuring resistors, which are advertised on internet, but our attempts to get them were unsuccessfully.

The purpose of this paper was to confirm the usability of this measuring method on high voltage and during 30 minutes came out the correctness of results listed in this paper.

TABLE I
MEASURING RESULTS

RESIDUAL OUTPUT

Observation	Predicted Y	Residuals
1	0.587398	0.002602
2	0.625066	0.002934
3	0.662733	-0.00473
4	0.705913	8.66E-05
5	0.761037	0.000963
6	0.810648	-0.00265
7	0.850153	-0.00215
8	0.891496	0.001504
9	0.939269	-0.00127
10	0.982449	0.001551
11	1.038491	-0.00049
12	1.085346	0.002602

Observation – input voltage u in kV; Predicted Y – output voltage in V; Residuals – measurement error in V.
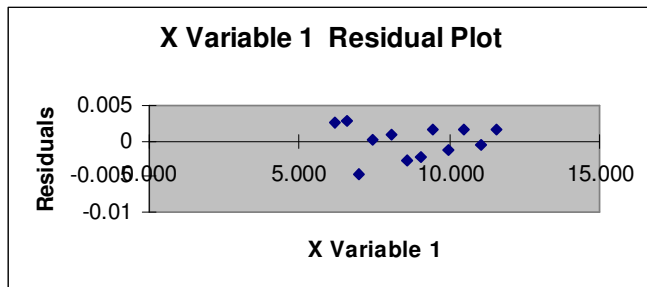
(Residuals – measurement error in V; x – input voltage u in kV)

Fig. 3. Graphical presentation of calibration results.
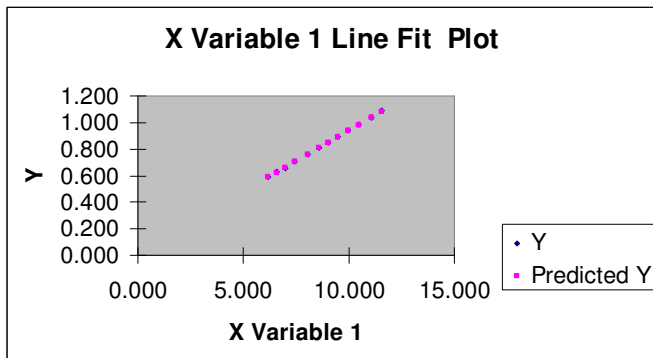
(Y – output voltage in volts; x – input voltage u in kV)

Fig. 4. Measurement results – scaled curve.

IV. DISCUSSION

The standard instrument has class 1, so the permissible reading error is 0.1%, and the standard deviation is (as a result of supplying the device from the mains –without stabilizer) about 0.5% during the measurement, hence arise that the measurement uncertainty is about 0.6%, that is in great extent in keeping with won nonlinearity. It is possible, that the nonlinearity is still higher. We are pointing out that the scale of instrument „S 196" is quadratic, so the reading error is 0.1% on the end of the scale, but on the half the scale is 0.4%, so that fact also confirms the conclusion that the linearity of the built instrument is better than the gained 0.5%.

V. CONCLUSION

In the paper, linear voltmeter for direct measurement of voltage on 20 kV net (11,5kV regarding to earth).

As the theory confirms and the experiment shows, it has high linearity.

The theory provides linearity from several ppm, while the experiment has showed linearity of 0.5 % , what is on the level of estimated measurement uncertainty for the applied measuring equipment. The result is encouraging and the investigation is going to be continued.

REFERENCES

[1] B. Santrač, M. Sokola, Z. Mitrović, I. Župunski, V. Vujičić " A Novel Method for Stochastic Measurement of Harmonics at Low Signal – to – Noise Ratio", IEEE Transactions on Instrumentation and Measurement, 2008, (accepted for publication)
[2] D. Čomić, S. Milovančev, V. Vujičić, "A New Approach to Voltage Measurements in Power System", 9th International Conference on Electrical Power Quality and Utilisation, Barcelona, October 2007
[3] N. Pjevalica "Merenje na elektrodistributivnoj mreži u frekvencijskom domenu", Doktorska teza, Fakultet tehničkih nauka u Novom Sadu, 2007.

Classification of Musical Audio Recordings

Igor Marić and Vladimir Risojević

Abstract—**In this paper, the automatic classification of musical audio recordings into a hierarchy of musical genres is explored. Three features sets for representing timbral texture, rhythmic content and pitch content of musical audio signals are reviewed. We give classification results using described features and a k-NN classifier. Accuracy of classification of 61% for ten musical genres is promising and this result is comparable to the results reported for human musical genre classification. We also analyzed the significance of individual features for classification and we show that timbral texture features yield the best results for this dataset.**

Index Terms—**Digital signal processing, music, musical genre, classification, audio recording.**

I. INTRODUCTION

THE creation of huge digital musical audio databases coming from both the restoration of existing analog archives as well as the creation of the new content is demanding reliable and fast tools for content analysis and description. These tools will enable searching, browsing, and interactive access to the musical content. In that context, musical genres are crucial descriptors since they have been widely used for years by music dealers and librarians to organize music catalogs, libraries, and stores. Musical genres are labels created and used by humans to explore similarities between musicians and compositions, as well as to organize musical collections. They have no strict definitions and boundaries as they arise through a complex interaction between the public, marketing, historical, and cultural factors. Despite their use, music genres remain a poorly defined concept, which makes the automatic classification problem a nontrivial task [1].

In this paper, an algorithm for automatic classification of musical audio recordings into a hierarchy of musical genres is proposed. The algorithm has two basic steps. The first step is the representation of an audio recording using features which are extracted using digital signal processing techniques. The second step is the classification of feature vectors into the predefined categories.

The paper is structured as follows. Features used for representation of musical audio recordings and their extraction are reviewed in Section II. Section III deals with the statistical evaluation of results of the proposed classifier and Section IV

contains the concluding remarks and directions for future research.

II. FEATURES OF THE AUDIO SIGNAL

To be able to classify an audio signal, it is necessary to represent the signal using features, which reflect certain characteristics of the signal in some domain, e.g. time or frequency. Extracted features are then used for training of the classifier, and classification of a new signal is done on basis of its features extracted using the same procedure. In this paper we used three types of features, namely: timbral texture features, rhythmic content features and pitch content features.

A. Timbral texture Features

Audio signals are non-stationary, i.e. their spectral characteristics are changing in time. Therefore, they are analyzed in short time intervals within which the signal can be considered stationary and its parameters constant. This time interval is called the *analysis window*. When intervals with different spectral characteristics are interchanged with certain regularity, we can talk about sound texture. To examine this phenomenon quantitatively, it is necessary to observe the signal in a longer interval, which is called the *texture window*. Texture window consists of several analysis windows and its duration is approximately one second. Research on human subjects has shown that humans need only three seconds of music recording to identify the music genre [2]. Thus, we may conclude that humans for recognition of musical genres use the musical texture, in addition to the other characteristics of audio signals.

The musical texture can be quantitatively described using the following features which are based on the spectral characteristics of the signal:

1) *Spectral Centroid* is computed for each analysis window. It is the center of gravity of the magnitude spectrum of the window computed via STFT:

$$C_t = \frac{\sum_{k=1}^{N} k \cdot M_t(k)}{\sum_{k=1}^{N} M_t(k)} \qquad (1)$$

where $M_t(k)$ is the magnitude of the Fourier transform in analysis window t and frequency bin k. Higher values of this feature correspond to more high frequencies in the analysis window. Value of the spectral centroid in music signal windows is greater than in voice signal windows, because musical instruments produce tones with higher frequencies than those of the human voice.

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2) *Spectral Rolloff* is defined as the frequency R_t below which 85% of the magnitude distribution is concentrated

$$\sum_{k=1}^{R_t} M_t(k) \approx 0.85 \cdot \sum_{k=1}^{N} M_t(k) \qquad (2)$$

The value of this feature is higher if more signal energy is contained in high frequencies.

3) *Spectral Flux* is defined as the squared difference between the normalized magnitudes of successive spectral distributions

$$F_t = \sum_{k=1}^{N} (N_t(k) - N_{t-1}(k))^2 \qquad (3)$$

where $N_t(k)$ and $N_{t-1}(k)$ are the normalized magnitudes of the Fourier transform in the current window *t*, and in the previous window *t-1*, respectively. Magnitude in each window is normalized with the sum of magnitudes at all frequencies in the current window. The spectral flux is a measure of the amount of local spectral change.

4) *Zero Crossings feature* is computed in the time domain. Its value is the number of zero crossings in the current window:

$$Z_t = \frac{1}{2} \sum_{m=1}^{M} \left| \operatorname{sgn}(x(m)) - \operatorname{sgn}(x(m-1)) \right| \qquad (4)$$

where $x(m)$ is the signal in the window *t*. This feature is higher for unvoiced than for voiced speech. In speech signal, windows of voiced and unvoiced speech are interchanged which means that windows with low and high values of this features are interchanged. On the other hand the number of zero crossings in the window for musical signals is pretty much constant.

5) *Low-Energy Feature* is defined as the percentage of *analysis windows* that have less RMS energy than the average RMS energy across the *texture window*. If there is a large number of "silent" analysis windows the value of this feature will be high. A large number of "silent" analysis windows is a characteristic of speech signals.

6) *Mel-Frequency Cepstral Coefficients:* Mel-frequency cepstral coefficients (MFCC) are perceptually motivated and they are frequently used in speech recognition systems. In order to compute MFCC we pass the signal through a filter bank with central frequencies uniformly distributed on a logarithmic transformed frequency axis. In this paper we used the ISP (Intelligent Sound Implementation) model implementation of MFCC [3].

Most of these features are time-variant, i.e. their value changes in analysis windows in which we consider the sound signal to be stationary. Spectral centroid, spectral rolloff, spectral flux, zero crossings, and MFCC are computed for each analysis window. Means and variances of these features are computed for each texture window. On the other hand, low energy feature is computed for a texture window and the value of this feature is added to the feature vector for a texture window. The signal is represented with a unique feature vector

which is a mean value of feature vectors for individual texture windows.

B. Rhythmic Content Features

Although rhythm as a music concept is easy to understand, it is not easy to define. Human perception of rhythm is a subjective experience, but basically rhythm has always been described as repetition of emphasized elements or segments within the whole composition. The regularity of rhythm, the relation of the main beat to subbeats, and relative strengths of subbeats and the main beat are some of the characteristics we would like to represent in a feature vector. To compute the feature vector, it is necessary to perform beat detection, and construct *beat histogram* (BH). The procedure for beat detection is based on the discrete wavelet transformation (DWT) and is illustrated in Fig. 1 [2].

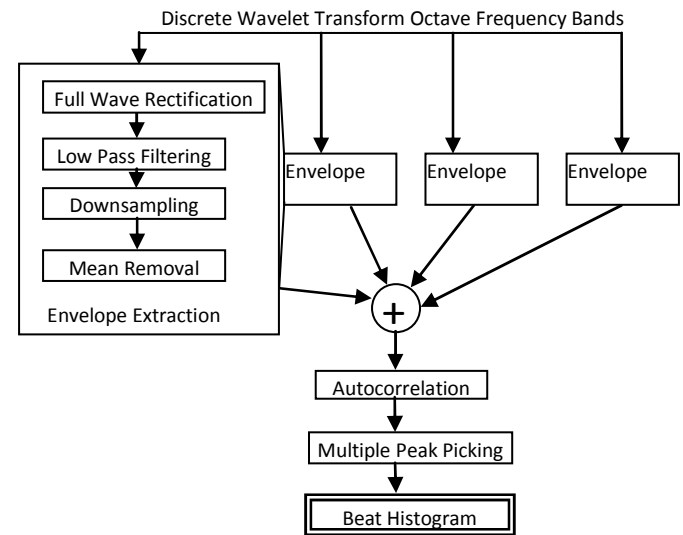The following signal processing techniques are used for beat analysis:

Fig. 1. Beat histogram calculation flow diagram.

1) *Full Wave Rectification:*

$$y(n) = |x(n)| \qquad (5)$$

is applied in order to extract the temporal envelope of the signal rather than the time domain signal itself.

2) *Low-Pass Filtering:*

$$y(n) = (1-\alpha) \cdot x(n) + \alpha \cdot y(n-1) \qquad (6)$$

using a one-pole filter with $\alpha = 0.99$ is used to smooth the envelope. Full wave rectification followed by low-pass filtering is a standard envelope extraction technique.

3) *Downsampling:*

$$y(n) = x(kn) \qquad (7)$$

where *k*=16 in our implementation. Because of the large periodicities for beat analysis, downsampling the signal reduces the computation time for the computation of the autocorrelation without affecting the performance of the algorithm.

4) *Mean Removal:*

$$y(n) = x(n) - E[x(n)] \qquad (8)$$

is applied in order to make the signal centered about zero for the autocorrelation stage.

5) *Enhanced Autocorrelation:*

$$y(n) = \frac{1}{N}\sum_n x(n) \cdot x(n-k).$$

(9)

is a method used to detect periodicities (similarities) in the signal, i.e. beat in our case. Rhythmic features are computed using Enhanced *Summary AutoCorrelation Function* (ESACF) [4].

In order to compute the ESACF we clip the sum of envelopes to positive values, upsample the result with factor 2, and subtract it from the original clipped function. The same process is repeated with other integer factors such that repetitive peaks at integer multiples of the main beat are removed. The first three peaks of the ESACF that are in the appropriate range for beat detection are selected and added to a *beat histogram (BH)*. The bins of the histogram correspond to beats-per-minute (bpm) from 60 to 220 bpm. Thus, peaks in the BH correspond to the self similarities of the signal.

Fig. 2 shows four beat histograms for 30s excerpts from different musical genres. In the upper left corner is a beat histogram of classics. This is a histogram of *Symphony No. 40* by Mozart.
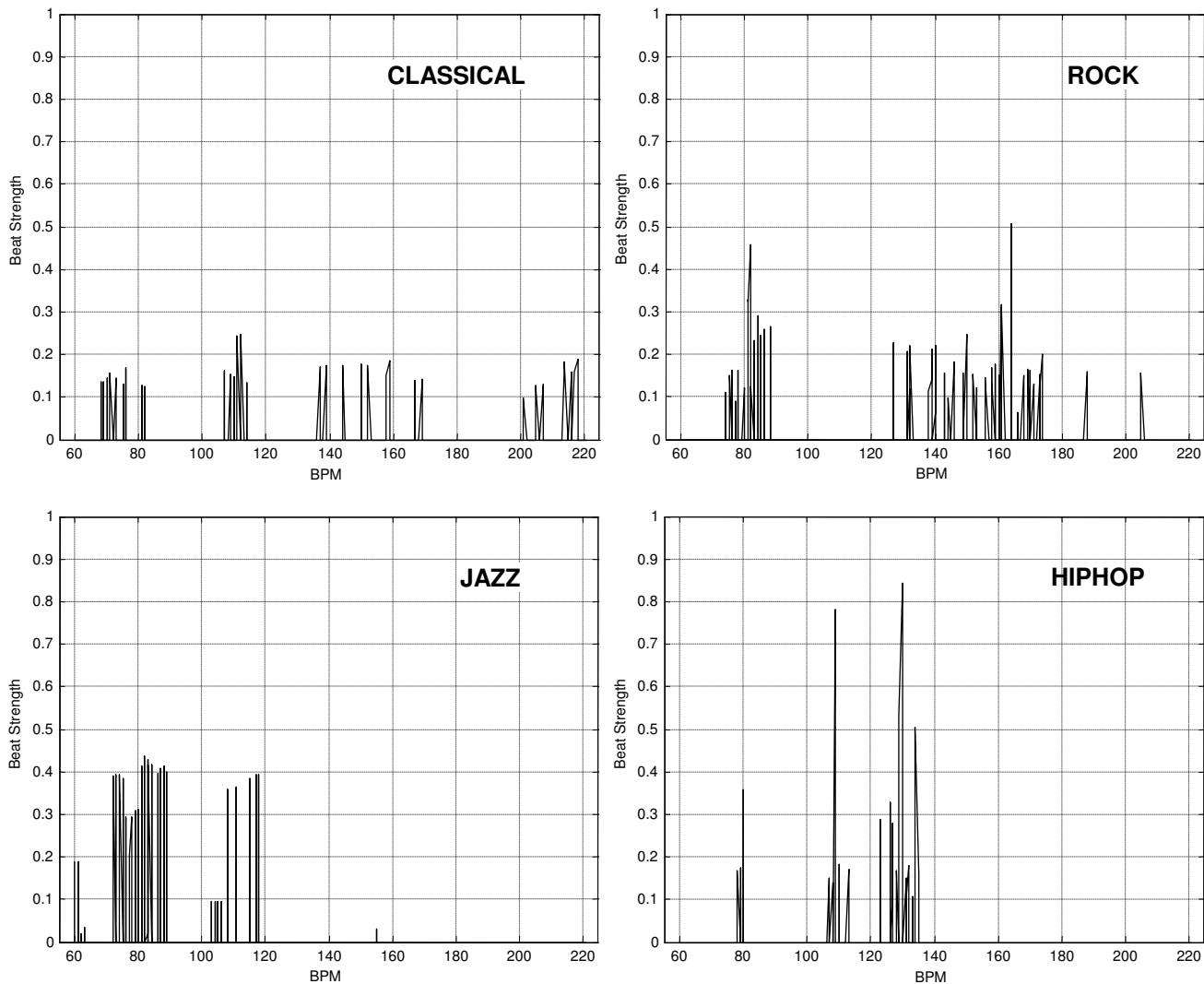
Fig. 2. Beat histogram examples.

We notice that in this composition there are no pronounced peaks in the histogram, as well as that the strength of the existing peaks is very low. This is a characteristic of the classical genre because of the complexity of multiple instruments in the orchestra, and because there is no pronounced rhythm section in classical music. Stronger peaks can be seen at the lower left, where the histogram for an excerpt from *I Can't Stop Loving You* by Ray Charles is shown. This composition belongs to the jazz genre. The values of the histogram are pretty much equal here, as well. There are peaks around 80bpm and 120bpm. In the upper right the histogram of a rock song *Come Together* by The Beatles is shown. Two largest peaks correspond to the mean beat, at approximately 80 bpm, and its first harmonic (twice the speed) at 160bpm. It is shown heuristically that the main beat usually corresponds to the first or second BH peak [2]. Peaks are more pronounced here, because the rock genre has stronger beat. The highest peaks in the lower right show strong rhythmical structure of the hip-hop song *Candy Shop* by 50Cent.

Fig. 2 indicates that the BH of different musical genres can be visually differentiated. The rhythm features include:

- **A0, A1**: relative amplitudes (divided by the sum of amplitudes) of the first and second histogram peak;
- **RA**: ratio of the amplitudes of the second and the first peak;
- **P1, P2**: periods of the first and second peak in bpm;
- **SUM**: overall sum of the histogram (indication of beat strength).

For the BH calculation, the DWT is applied to a window of 65 536 samples with a sampling rate of 22 050 Hz, which corresponds to approximately 3 s. This window is advanced by a hop size of 32 768 samples. This larger window is necessary to capture the signal repetitions at the beat and subbeat levels.

C. Pitch Content Features

In systems for audio analysis, pitch content is most often expressed by means of a Pitch Histogram (PH) [2]. PH is a statistical representation of the pitch content. Characteristics of tonality extracted from the PH form a set of tonality features. PH shows the number of appearances of each tone (note) in the musical audio recording. Histogram bins correspond to musical notes labeled using the MIDI note numbering scheme. Genres with more complex sound structures such as jazz or classical music tend to have a higher degree of pitch change than genres with simple chord progressions such as rock or pop music. As a consequence, pitch histograms for pop or rock music will have fewer and more pronounced peaks than the histograms of jazz or classical music. Algorithm for the calculation of PH is known under the name *Multiple Pitch Detection Algorithm* [4]. This algorithm is based on the model of two-channel pitch analysis. Block diagram of this model is shown in Fig. 3. Periodicity is detected by means of the autocorrelation function computed using:

$$x_2 = IDFT\left(\left|DFT(x_{low})\right|^k + \left|DFT(x_{high})\right|^k\right) \quad (10)$$

where x_{low} and x_{high} are signals before periodicity detection in lowpass and highpass channels, respectively, and DFT and IDFT indicate discrete Fourier transform and its inverse. The parameter k determines the frequency domain compression (for standard autocorrelation $k=2$, optimal $k=0.67$). Values obtained from (10) are used to calculate ESACF, as described in Section IIB for BH. Three dominant peaks of the ESACF in each analysis window are added to the histogram. The values of the histogram will be the highest when these peaks match. The frequencies corresponding to each histogram peak are converted to musical pitches such that each bin of the PH corresponds to a musical note with a specific pitch. The musical notes are labeled using the MIDI note numbering scheme. The conversion from frequency to MIDI note number can be performed using

$$n = 12\log_2\left(\frac{f}{440}\right) + 69 \quad (11)$$

where *f* is frequency in Hertz and *n* is the histogram bin (MIDI note number).
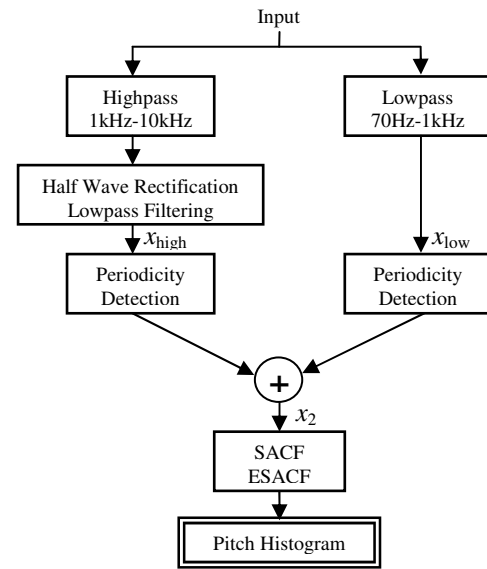

Fig.3. Multiple Pitch Detection Algorithm.

Two versions of the PH are created: *folded* (FPH) and *unfolded* histogram (UPH). The UPH is created using the equation (11). In the folded case, all notes are mapped to a single octave using

$$c = n \cdot \bmod 12 \quad (12)$$

where *c* is the folded histogram bin (pitch class), and *n* is the unfolded histogram bin (or MIDI note number). Finally, the FPH is mapped to a circle of fifths histogram so that adjacent histogram bins are spaced a fifth apart rather than a semitone. This mapping is achieved by

$$c' = (7 \cdot c) \bmod 12 \quad (13)$$

where c' is the new folded histogram bin after the mapping and *c* is the original folded histogram bin. The number seven

corresponds to the seven semitones in a music interval of a fifth. That way, the distances between adjacent bins after the mapping are better suited for expressing tonal music relations (tonic-dominant) and the extracted features result in better classification accuracy. So, FPH contain information related to the music tonality content while UPH defines the range of tones.

PHs for examples from the jazz and rock genres are given in Fig. 4 and 5. We can see that rock music has fewer and more pronounced peaks in the histogram than jazz. This is a consequence of the fact that genres such as jazz or classical have a wider range of tonality than genres such as rock or pop.

The following features are computed from the UPH and FPH in order to represent pitch content:
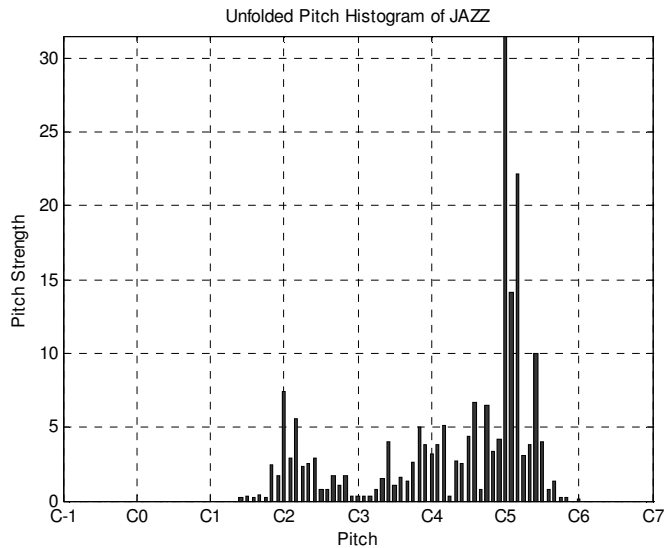
Fig. 4. UPH example for Jazz.
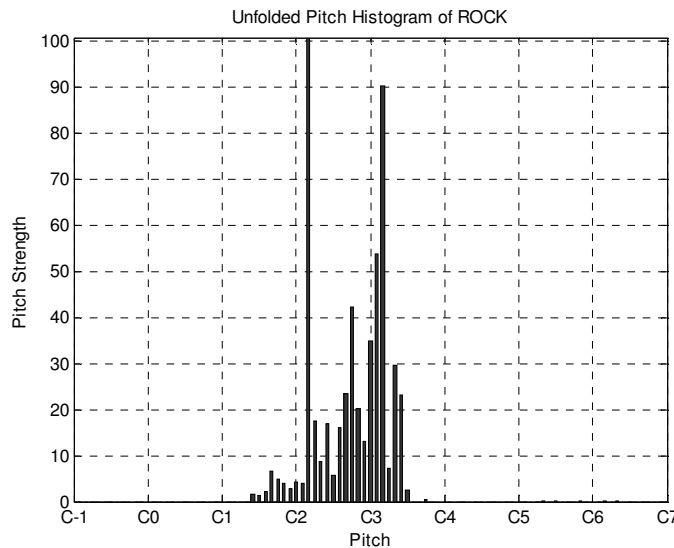
Fig. 5. UPH example for Rock.

- **FA0**: Amplitude of the maximum peak of the folded histogram. This corresponds to the most dominant pitch of the song. For tonal music this peak will typically

correspond to the tonic or dominant chord. This peak will be higher for songs that do not have many harmonic changes.

- **UP0**: Period of the maximum peak of the unfolded histogram. This corresponds to the octave range of the dominant musical pitch of the song.
- **FP0**: Period of the maximum peak of the folded histogram. This corresponds to the main pitch class of the song.
- **IPO1**: Pitch interval between the two most prominent peaks of the folded histogram. This corresponds to the main tonal interval relation. For pieces with simple harmonic structure this feature will have value 1 or -1 corresponding to fifth or fourth interval (tonic-dominant).
- **SUM** The overall sum of the histogram. This is feature is a measure of the strength of the pitch detection.

For the computation of the PH, a pitch analysis window of 512 samples at 22 050 Hz sampling rate (approximately 23 ms) is used.

III. CLASSIFICATION OF AUDIO RECORDINGS

The test collection used in this paper consists of 1000 audio records. Each audio record is 30s long and recorded mono with 16 bits and sampling rate of 22050 Hz. Audio recordings contain music from 10 different genres whose hierarchy is shown in Fig. 6. Some of the musical examples are instrumental, and some include vocals. Used audio recordings are of different quality because they are collected from CDs, radio and the Web. This collection is also used in paper [2].

For classification we used a *K*-nearest neighbor (*k*-NN) classifier with Mahalanobis distance. 10-fold cross-validation algorithm is used for testing [6].
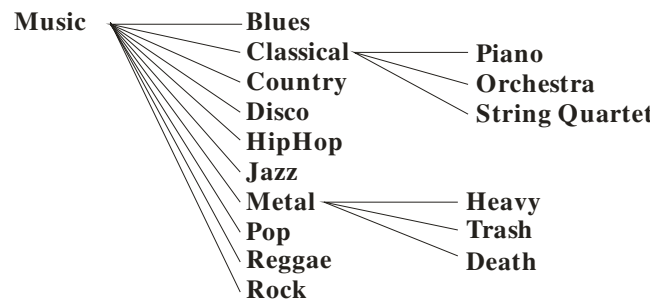
Fig. 6. Hierarchy of musical genres.

A. Classification Results

Total classification accuracy for ten musical genres is 61%. Percentages of examples which are classified correctly genre-wise are shown in Fig. 7. It can be seen that the classical music as a unique genre yields the best classification accuracy of 90%. Metal as a unique genre is another notable example. The lowest accuracy is obtained for rock genre, which can be explained by its relations to other genres. Table 1 provides a detailed insight into the classification of musical genres in the form of a confusion matrix Columns of this matrix correspond to the actual genres and its rows to the predicted genres. For

example, cell in the 6th row and 2nd column has a value of 7, which means that 7% of *classical* music (column 2) is incorrectly classified as *jazz* (row 6). Percents of correctly classified genres are given on the diagonal of the matrix.
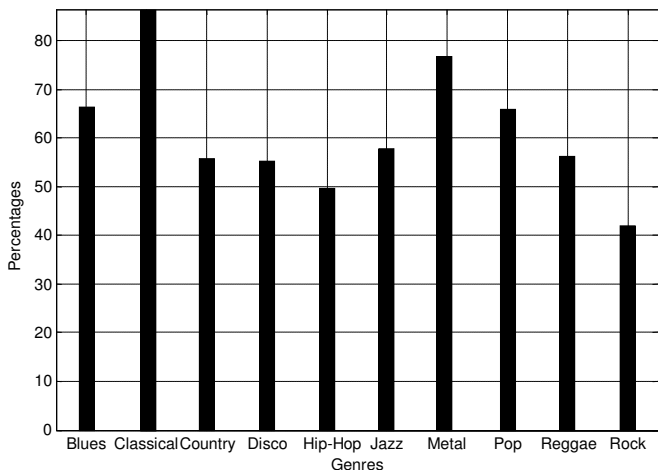

Fig. 7. Classification accuracy percentages.

Confusion matrix shows that the errors in the classification are similar to what a human would do. For example, *classical* music is classified as *jazz* in compositions that have strong rhythm, as in the works of Leonard Bernstein and George Gershwin.

TABLE I
GENRE CONFUSION MATRIX

	cl	co	di	hi	ja	ro	bl	re	po	me
cl	**67**	1	5	4	6	9	2	2	7	7
co	0	**87**	2	1	0	12	0	0	0	2
di	8	1	**56**	7	1	13	2	6	6	17
hi	3	1	5	**55**	11	1	2	7	5	7
ja	3	0	1	6	**50**	2	5	6	10	1
ro	7	7	9	1	1	**58**	0	3	1	2
bl	2	1	2	3	3	0	**77**	1	0	13
re	0	0	1	11	7	1	0	**66**	9	5
po	1	0	4	5	19	0	0	3	**56**	4
me	9	2	15	7	2	4	12	6	6	**42**

Blues genre overlaps with *jazz*, *rock* and *country* music, *country* with *jazz* and *rock*, *reggae* with *hip-hop*, etc. As mentioned, *rock* music has the worst classification accuracy and is easily confused with other genres, which is expected because of its broad nature. The confusion matrix for subgenres of the *classical* genre is given in Table II. Overall classification accuracy is 78%, which is good. It can be seen from the confusion matrix that the *orchestral music* is incorrectly classified as a *string quartet* in 28% of the cases, which is expected if you take into account that most orchestras usually include string instruments.

Confusion matrix in Table 3 presents the results of classification of the subgenres of the *metal* genre. Overall classification accuracy is 65%. Classification accuracy of the

d*eath* metal subgenre is notable. This subgenre is easily distinguished by the specific style of singing and the color of the voice, as well as by melody and the way of playing.

TABLE II
CONFUSION MATRIX OF SUBGENRES OF THE CLASSICAL GENRE

	Piano	Orchestra	String Quartet
Piano	82	0	8
Orchestra	1	72	11
String Quartet	17	28	81

Heavy and *trash* metal are largely overlapping. It can be said that the *trash* contains *heavy* and vice versa, because *heavy* is the root of the *metal* music.

TABLE III
METAL CONFUSION MATRIX

	Heavy	**Trash**	**Death**
Heavy	**68**	**51**	**7**
Trash	**23**	**46**	**11**
Death	**9**	**2**	**82**

Table 4 shows the classification accuracy of *k*-NN classifiers for different values of the parameter *k* applied to the three sets of musical genres. Means and standard deviations of correctly classified examples in cross-validation are given. In the first row of the table the results for random classification are given.

TABLE IV
CLASSIFICATION ACCURACY MEAN AND STANDARD DEVIATION

	Genres(10)	**Classical(3)**	**Metal(3)**
Random	**10**	**33**	**33**
*k*NN(1)	58 ± 1	78 ± 5	55 ± 8
*k*NN(3)	61 ± 1	72 ± 4	65 ± 6
*k*NN(5)	60 ± 1	67 ± 8	54 ± 6
*k*NN(7)	60 ± 1	59 ± 6	52 ± 4

In Table V the individual importances of the proposed feature sets in the automatic classification of musical genres are given. Classification is done for *k* = 3. The first row in the table is random classification, while the last line corresponds to the full set of features. Numbers in brackets behind the labels of features represent are numbers of features for that individual set.

TABLE V
INDIVIDUAL FEATURE SET IMPORTANCE

	Genres(10	**Classical(3)**	**Metal(3)**
RND	**10**	**33**	**33**
PHF(5)	**35**	**48**	**48**
BHF(6)	**24**	**46**	**55**
STFT(9)	**45**	**56**	**44**
MFCC(10)	**59**	**70**	**54**
FULL(30)	**61**	**72**	**65**

As can be seen, features that are not based on the timbral texture but on pitch content (Pitch Histogram Features-PHF) and rhythm content (Beat Histogram Features-BHF) give worse results than the features based on the texture (STFT, MFCC) except in the case of the metal genre, where they perform approximately the same. Since the metal music is very melodic, rhythmic, harmonious and rapid greater accuracy is obtained using pitch and rhythm features. In all cases, the proposed set of features gives better results than random classification, which means that certain features give information about musical genres and musical content in general. The classification accuracy of the combined feature set (FULL(30)) in some cases is not significantly better compared to the classification accuracies of the individual feature sets. This fact does not necessarily imply that the features are correlated or do not contain useful information because it is possible that a specific file is correctly classified by two different feature sets that contain different and uncorrelated feature information. In addition, although certain features are correlated, the addition of each specific feature improves the classification accuracy. The rhythmic and pitch content features seem to play a less important role in the classification of the *classical* and *metal* datasets compared to the *genre* dataset. This is an indication that it is possible that *genre* datasets needs to be organized in a deeper hierarchy of subgenres.

IV. CONCLUSIONS AND FUTURE WORK

Despite the fuzzy nature of genre boundaries, classification of musical audio recordings can be performed automatically with the accuracy that can be compared to human classification.

Three feature sets for representing timbral texture, rhythmic content and pitch content of music signals are computed and used for classification of musical audio recordings using a *k*-NN classifier, which was tested on a large collection of various audio recordings. Using the presented feature set classification accuracy of 61% has been achieved on a dataset consisting of ten musical genres, as well as 78% and 65% on *classical* and *metal* datasets.

We also evaluated the importance of individual feature sets for the classification of musical audio recordings. Furthermore, we examined the performance of the *k*-NN classifier, i.e. the mean and the standard deviation of the percentage of correctly classified examples, as a function of the parameter *k*, which affects the voting in the nearest neighbor algorithm. The success of the proposed features for musical genre classification reveals their potential for other tasks such as similarity retrieval, segmentation and audio thumbnailing.

In further work we plan to additionally improve the features, and even add new ones, as well as to work on improving the algorithms for their extraction. From the analysis of the results we believe that the genre hierarchy should be expanded both in width and depth. Two additional sources of information about the musical genre are the melody and the singer voice. Also in the future research the attention should be paid to other semantic descriptors such as the emotions and the style of singing. More research of the pitch content features could also possibly lead to better performance.

REFERENCES

[1] N. Scaringella, G. Zoila, and D. Mlynek, "Automatic Genre Classification of Music Content," *IEEE Signal Processing Magazine*, Vol. 23, No. 2, pp. 133-141, 2006.

[2] G. Tzanetakis and P. Cook, "Musical Genre Classification of Audio Signals," *IEEE Transactions on Signal Processing*, Vol. 10, No. 5, 2002.

[3] S. Sigurdsson, K. B. Petersen, and T. Lehn-Schiøler, "Mel Frequency Cepstral Coefficients: An Evaluation of Robustness of MP3 Encoded Music," in *Proc. 7th International Conference on Music Information Retrieval, ISMIR 2006*, Victoria, Canada, 2006, pp. 286-289.

[4] T. Tolonen and M. Karjalainen, "A Computationally Efficient Multipitch Analysis Model," *IEEE Transactions on Speech and Audio Processing*, Vol. 8, No. 6, pp. 708-716, November 2000.

[5] D. Despić, *Teorija Muzike*, Zavod za udžbenike, Beograd, 2007.

[6] R. O. Duda, P. E. Hart, and D. G. Stork, *Pattern Classification*, John Wiley & Sons, Inc., 2001.

Influence of Imperfect Carrier Signal Recovery on Performance of SC Receiver of BPSK Signals Transmitted over α-μ Fading Channel

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Abstract—**This paper presents the analysis of the reception of binary phase-shift keying (BPSK) signals transmitted over the generalized α-μ fading channel. The selective combining (SC) and then demodulation and detection of the input signal are performed in the receiver while the estimation of the received signal phase is imperfect. We determine the BER dependence on the simultaneous influences of the imperfect reference signal recovery, number of diversity branches, fading severity and average signal-to-noise ratio in the channel.**

Index Terms—**Diversity systems, Error probability, Fading, Phase-shift keying, Probability density function.**

I. INTRODUCTION

IN wireless systems, the variation of instantaneous value of the received signal, i.e. fading of the signal envelope is very common effect, due to the multipath propagation. Fading is one of the main causes of performance degradation in wireless communication systems [1-10].

Diversity technique is certainly one of the most frequently used methods for combating the deleterious effect of channel fading and increasing the communication reliability without enlarging either transmitting power or bandwidth of the channel. The outline of this technique is that the same information is transmitted over few different non-correlated channels. In that way the influence of the fading onto each particular channel is independent. Signals from different channels are, then, combined in order to obtain the resulting signal. In that way the influence of the fading is mainly reduced. Particular diversity methods and combining techniques are presented in [1]-[7]. Selective combining (SC) is combining technique where the strongest signal is chosen among L branches of diversity system.

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The criterion for the selection of the branch is the largest value of instantaneous signal-to-noise ratio among the branches [1]-[3], [6], [7], [10]. Unlike of equal-gain-combining and maximum-ratio-combining techniques, a cophasing in the receiver is not required in SC technique, because, only one branch, one with the best characteristics in that precise moment, is chosen. Although SC technique brings the smallest improvement of receiver performances, the simplicity of practical realization makes the mentioned technique widely spread [1]-[3], [6], [7]. That is the reason why all the calculations for receiver performances in this paper will be presented for SC technique at the reception.

The generalized α-μ fading model was recently proposed in [11], [12] by considering two parameters, namely non-linearity and clustering. The α-μ distribution is written in terms of physically-based fading parameters, namely α and μ, which describe the non-linearity (α) of propagation medium and the multipath wave clustering (μ). This distribution includes the Rayleigh, Nakagami-m, Weibull, and Lognormal distribution as special cases.

Aalo et al. [13] presented a closed-form expression for the average bit error probability for both coherent and noncoherent/differentially coherent binary digital modulations in the generalized Gamma fading channel. Reference [14] considered the performance of linear diversity reception schemes over generalized gamma fading channels under assumption of perfect reference signal extraction.

The phase-locked loop (PLL) is used for carrier signal recovery from non-modulated signal in the receiver. As the receiver is not ideal, a certain phase error appears. The phase error is a difference between the phase of the incoming signal and the phase of the recovered carrier signal in the loop, and this may lead to serious degradation to system performance. It is a statistical process which follow Tikhonov distribution [4], [5], [15]. To the best of our knowledge, the performance of SC receivers of binary phase-shift keying (BPSK) signals in generalized gamma (α-μ) fading in the presence of the imperfect reference signal extraction has not been examined.

In the following, the analysis of the BPSK signal detection over α-μ fading channel is presented. The selective combining of the signals from L branches is performed before the detection. The analysis is performed considering that the

carrier signal extraction is imperfect. The analytical expressions for probability density function (PDF) of the signal envelope are determined, as well as the expressions for the average bit error rate (BER) in detection. Using these expressions, the dependence of average BER on average signal-to-noise ratio is obtained for different number of diversity branches L and different standard deviations σφ of phase error. The influence of the α-μ fading parameters on the average BER is determined. Also the graphs which represent the dependence of average BER on σ_φ are shown.

II. MODEL OF SYSTEM

We shall initially introduce a transmitter which sends digitally binary phase-modulated signal in a form $A\cos(\omega_0 t + \Phi_0)$. Depending on a sent symbol, Φ_0 can take following values from the set $\Phi_0 \in \{0, \pi\}$. After the propagation through the fading channel, signal at the k-th branch has the form (Fig. 1):

$$z_k(t) = r_k(t)\cos(\omega_0 t + \Phi_0 + \delta_k(t)) + n_k(t) \tag{1}$$

where $r_k(t)$ is the envelope of the received signal, ω_0 the angular frequency of the carrier, Φ_0 is the transmitted phase of the signal, $\delta_k(t)$ is the random phase (the phase noise caused by multipath fading), and $n_k(t)$ is the additive white Gaussian noise in the k-th diversity branch with zero mean value and variance σ^2. It is assumed that the noise power is same in every diversity branch and fading is uncorrelated among different branches.

Regarding the above mentioned assumption, the chosen branch in the combining circuit is the one in which the envelope of the received signal has the largest value. As it is shown in Fig. 1, the signal envelope at the output of the combining circuit is:

$$r_i(t) = \max\{r_1(t), r_2(t), ..., r_k(t), ..., r_L(t)\} \tag{2}$$

After the combining, signal is first led to the band-pass filter (BPF) with central frequency f_0. The filtered signal is then multiplied by the signal from the estimator of reference carrier. Resulting signal is next led into the low-pass filter (LPF) and sampled in moments $t=t_0$. Finally, on the basis of the sampled value $r_i(t_k)\cos(\Phi_0 + \varphi(t_k))$ decision block determines which phase of the signal is transmitted.

a)

b)
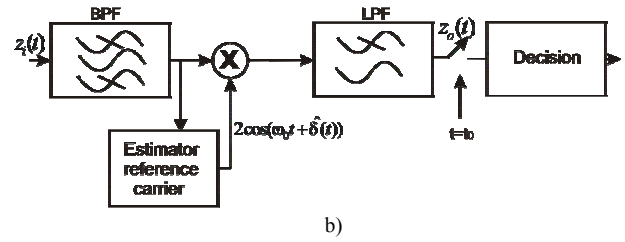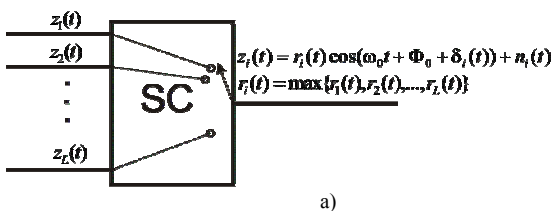
Fig. 1. (a) Selection combining and (b) signal detection of BPSK signals.

The purpose of the PLL is to estimate the phase of the incoming signal. In ideal case, the estimated phase should be equal to the phase of the incoming signal $\delta_i(t)$. However, in practical realizations there is certain disagreement between the estimated phase $\hat{\delta}(t)$ and the phase of the signal $\delta_i(t)$. This disagreement is phase error and it is expressed as $\varphi(t) = \delta_i(t) - \hat{\delta}(t)$. The PDF for this phase error corresponds to Tikhonov distribution [4], [5], [15]:

$$p_\varphi(\varphi) = \frac{e^{\alpha_{PLL} \cdot \cos\varphi}}{2\pi \cdot I_0(\alpha_{PLL})}, \quad -\pi \le \varphi < \pi \tag{3}$$

where the parameter α_{PLL} represents the signal-to-noise ratio in the PLL circuit and gives the information about the preciseness of phase estimation of incoming signal. It can be assumed $\alpha_{PLL} = 1/\sigma_\varphi^2$, where σ_φ is a standard deviation of the phase error [4], [5], [15]. The modified Bessel function of the first kind and order zero is denoted by $I_0(\cdot)$ [16, eq. (8.406)].

The PDF of the signal envelope at the output of the combining circuit with L branches can be written as [3]:

$$p_{r_i}(r_i) = L \cdot p_r(r_i)\left(\int_0^{r_i} p_r(t)dt\right)^{L-1} \tag{4}$$

where $p_r(r)$ is the PDF of the signal envelope at the k-th branch. Since the envelopes of the signals in these branches underlying α-μ distribution with same characteristics the expression (4) can be written as:

$$p_{r_i}(r_i) = L \cdot \frac{\alpha \cdot \mu^\mu \cdot r_i^{\alpha\mu-1}}{\hat{r}_i^{\alpha\mu} \cdot \Gamma(\mu)} \cdot \exp(-\mu\frac{r_i^\alpha}{\hat{r}_i^\alpha})\left(\int_0^{r_i} \frac{\alpha \cdot \mu^\mu \cdot t^{\alpha\mu-1}}{\hat{t}^{\alpha\mu} \cdot \Gamma(\mu)} \cdot \exp(-\mu\frac{t^\alpha}{\hat{t}^\alpha})dt\right)^{L-1} \tag{5}$$

After the classical analysis of the signal detection [9], [10], the expression for the conditional BER for BPSK signal, as a function of signal-to-noise ratio in the channel $\gamma = \frac{r_i^2}{2\sigma^2}$, $\sigma^2 = \overline{n^2(t)}$ and phase error φ, can be presented as:

$$P_{e/\varphi,\gamma} = \frac{1}{2}\text{erfc}(\sqrt{\gamma}\cos\varphi). \tag{6}$$

The average BER is:

$$BER = \frac{1}{2} \int_{-\pi}^{\pi} \int_{0}^{\infty} \operatorname{erfc}\left(\sqrt{\gamma} \cos\varphi\right) \cdot L \cdot \frac{\alpha}{2\Gamma(\mu)} \cdot \left(\frac{\Gamma\left(\mu + \frac{2}{\alpha}\right)}{\Gamma(\mu)}\right)^{\frac{\alpha\mu}{2}} \cdot \frac{\gamma^{\frac{\alpha\mu}{2}-1}}{\overline{\gamma}^{\frac{\alpha\mu}{2}}} \cdot$$

$$\cdot \exp\left(-\left(\frac{\gamma}{\overline{\gamma}} \cdot \frac{\Gamma\left(\mu + \frac{2}{\alpha}\right)}{\Gamma(\mu)}\right)^{\frac{\alpha}{2}}\right) \cdot \left(\int_{0}^{\sqrt{\frac{\gamma}{\overline{\gamma}} \cdot \frac{\Gamma\left(\mu + \frac{2}{\alpha}\right)}{\Gamma(\mu)}} \mu^{-\frac{2}{\alpha}}} \frac{\alpha \cdot \mu^{\mu}}{\Gamma(\mu)} \cdot u^{\alpha\mu-1} \cdot e^{-\mu u^{\alpha}} du\right)^{L-1} \quad (7)$$

$$\cdot \frac{e^{\alpha_{PLL} \cdot \cos\varphi}}{2\pi \cdot I_0(\alpha_{PLL})} \cdot d\gamma \cdot d\varphi$$

where is $\overline{\gamma}$ the average signal-to-noise ratio, γ is the instantaneous signal-to-noise ratio, $\log_2(\cdot)$ is the logarithm to base 2, $\operatorname{erfc}(\cdot)$ is the complementary error function [16, eq. (7.1.2.)], and $\Gamma(.)$ is the gamma function [16, eq. (8.310/1)].

III. NUMERICAL RESULTS

Using (7), one can calculate the average BER for α-μ fading channel and discuss performances of the receiver for different values of α and μ parameters, standard deviation of phase noise, σ_φ, as well as for different number of diversity branches L.

The influence of diversity order on the performances of the receiver can be observed from Fig. 2 where dependence of the average BER on average signal-to-noise ratio ($\overline{\gamma}$) is shown for different values of parameter L. The $\overline{\gamma}$ is marked as γ_{sr} in all figures.   With the increase of the diversity order, performances of the receiver improve. However, larger number of diversity branches reduces the additional gain and increases the complexity of the system. Therefore, it is necessary to find a compromise between the performances of the system and its complexity. Power gain is the highest when order of diversity system changes from $L = 1$ to $L = 2$. For example, in order to obtain the same value of BER=10^{-4}, for parameter values α=2.5, μ=1.5, and σ_φ=5°, it is necessary for average signal-to-noise ratio to reach the value of $\overline{\gamma} = 19{,}45$ dB for $L = 1$, $\overline{\gamma} = 11{,}8$ dB for $L = 2$, $\overline{\gamma} = 9{,}5$ dB for $L = 3$, $\overline{\gamma} = 8{,}4$ dB for $L = 4$, $\overline{\gamma} = 7{,}7$ dB for $L = 5$, and $\overline{\gamma} = 7{,}25$ dB for $L = 6$. It can be noticed that the gain exponential declines with the increase of the order of diversity system. In Table 1 calculated power gains are presented in decibels.
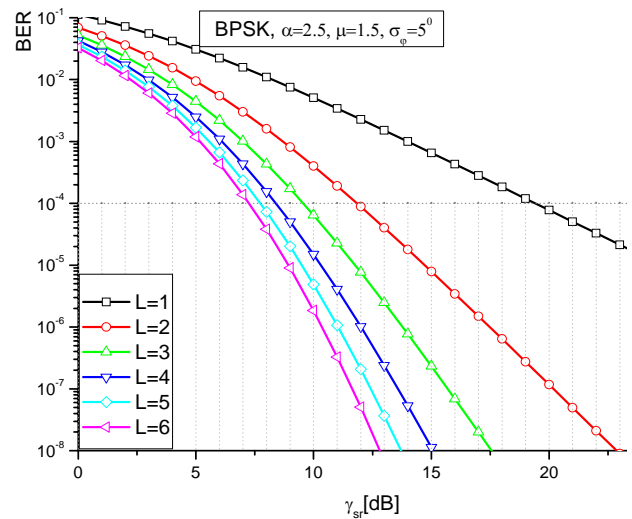
Fig. 2. Influence of diversity order on BER performance.

TABLE I
GAIN OF THE AVERAGE SIGNAL-TO-NOISE RATIO FOR DIFFERENT DIVERSITY ORDERS (FOR BER=10^{-4})

Crossing from lower to higher of diversity order L	Gain $\overline{\gamma}$
from L=1 to L=2	7,65 dB
from L=2 to L=3	2,30 dB
from L=3 to L=4	1,10 dB
from L=4 to L=5	0,70 dB
from L=5 to L=6	0,45 dB

The influence of the carrier extractor quality (the σ_φ value) on the performances of BPSK receiver is presented in Fig. 3. One can notice that for larger values of $\overline{\gamma}$, the irreducible error floor (BER floor) appears. Therefore, no increase of $\overline{\gamma}$ can cause the BER to fall under the certain value.   It is because some of the received bits can be wrongly detected, due to the error in PLL, even when the power of additive Gaussian noise is approaching zero.

The BER dependence on the average signal-to-noise ratio is shown in Fig. 4 for different values of fading parameters α (Fig. 4 (a)) and μ (Fig. 4 (b)) with diversity order $L = 4$ and $\sigma_\varphi = 5°$.

Fig. 5 presents the dependence of the BER on the fading parameters α (Fig. 5 (a)) and μ (Fig. 5 (b)) for different values of the average signal-to-noise ratio and constant values of the diversity order L=2 and phase noise standard deviation $\sigma_\varphi = 5°$.

The dependence of the average BER on the phase noise standard deviation is shown in Fig. 6, while the average signal-to-noise ratio is used as a parameter. In Fig. 6 it can be seen that the curves of the BER dependences on the phase noise standard deviation are approximately constant for the σ_φ values up to 13^0.
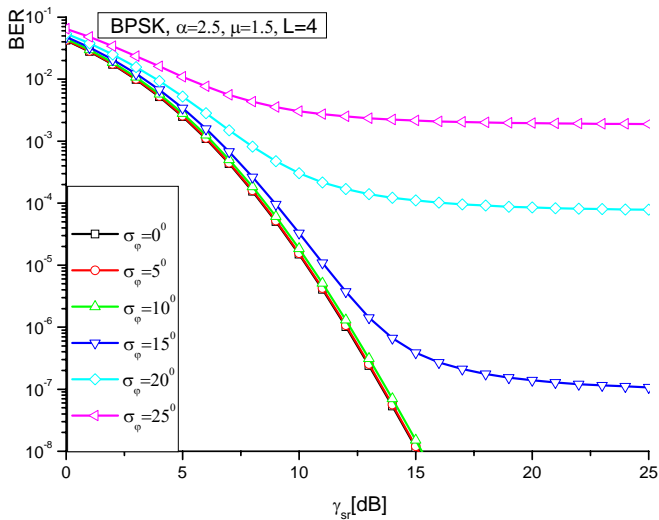
Fig. 3. Influence of carrier extractor quality on BER performance.

(a)

(a)

(b)
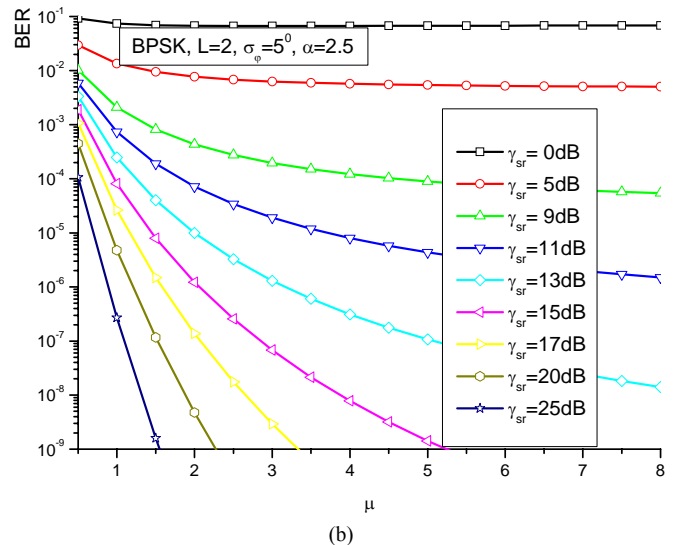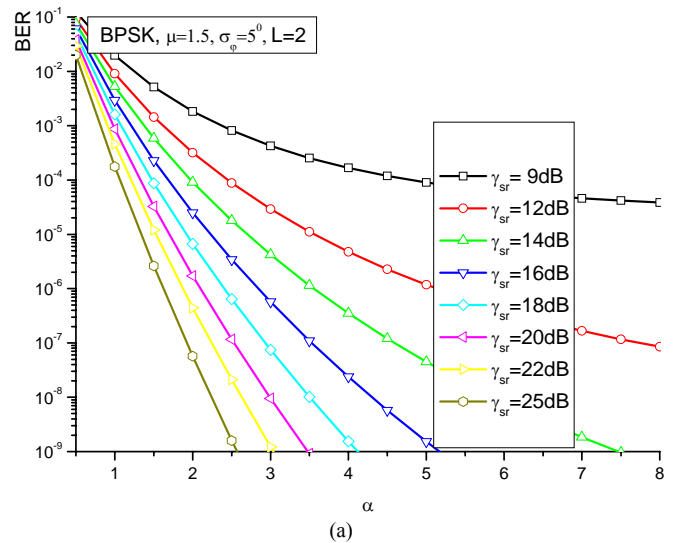
Fig. 5. Dependence of average BER on fading parameters α (a) and μ (b) for different values of average signal-to noise ratio.
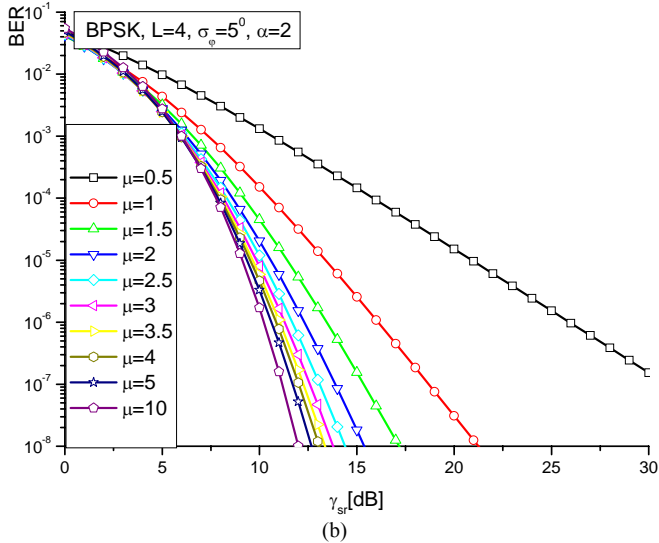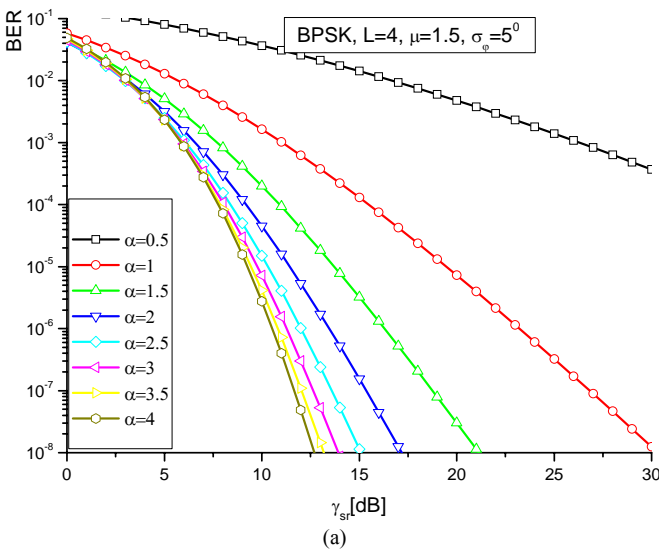

(b)

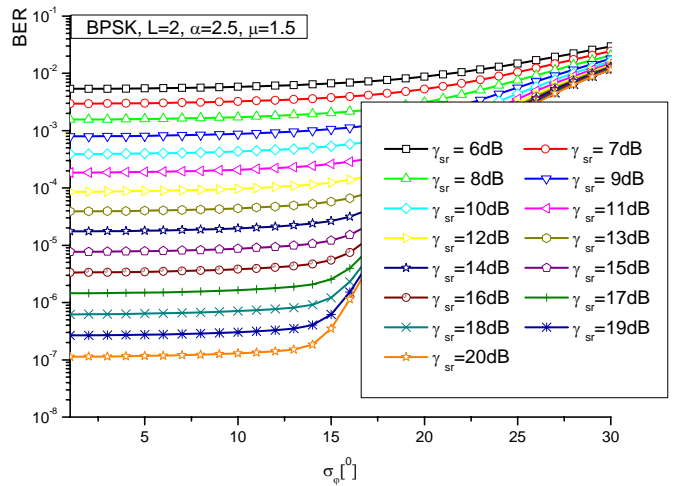Fig. 4. Influence of fading parameters: (a) α and (b) μ on the performances of the receiver.

Fig. 6. Dependence of average BER on phase noise standard deviation for different values of average signal-to-noise ratio.

IV. CONCLUSION

From the previously performed analysis of selective combining of BPSK signal over α-μ fading channel, the BER is determined in the presence of the imperfect reference carrier extraction. On the basis of presented results it can be concluded in which measure standard deviation of the phase error has the influence on the performances of the receiver. It is shown that the stochastic phase error yields a BER floor. This BER floor is determined for different values of phase error standard deviation. Furthermore, the influence of number of diversity branches on the performances of the system was examined and it is established how much the value of the BER is reduced with the increase of the number of branches. Obtained results enable one to find a compromise between the efficiency (which is measured by the value of BER) and the complexity of the receiver (measured by the number of receiving antennas). More detailed comments on these results are presented in previous part of this paper.

REFERENCES

[1] M. K. Simon, M. S. Alouini, *Digital Communication over Fading Channels: A Unified Approach to Performance Analysi.* John Wiley & Sons, Inc. 2000.

[2] J. D. Parsons, *The Mobile Radio Propagation Channel.* Second Edition, John Wiley & Sons Ltd 2000.

[3] Z. J. Mitrović, "Diversity Systems and Signal Detection by Receivers with Multiple Antennas," Diploma paper, Faculty of Electronic Engineering, Niš, August, 2007, (in Serbian).

[4] M. A. Najib, V. K. Prabhu, "Analysis of Equal-Gain Diversity with Partially Coherent Fading Signals," *IEEE Transactions on Vehicular Technology,* Vol. 49, No. 3, pp. 783-791, May 2000.

[5] N. C. Sagias, G. K. Karagiannidis, "Effects of Carrier Phase Error on EGC Receivers in Correlated Nakagami-m Fading," *IEEE Communications Letters,* Vol. 9, No. 7, pp. 580-582, July 2005.

[6] E. A. Neasmith, N. C. Beaulieu, "New Results on Selection Diversity," *IEEE Transactions on Communications,* Vol. 46, No. 5, pp. 695-704, May 1998.

[7] Q. T. Zhang, H. G. Lu, "A General Analytical Approach to Multi-Branch Selection Combining Over Various Spatially Correlated Fading Channels," *IEEE Transactions on Communications,* Vol. 50, No. 7, pp. 1066-1073, July 2002.

[8] J. Sun, I. S. Reed, "Performance of MDPSK, MPSK, and Noncoherent MFSK in Wireless Rician Fading Channels," *IEEE Transactions on Communications,* Vol. 47, No. 6, pp. 813-816, June 1999.

[9] D. Drajić, *Introduction to Statistical Telecommunication Theory.* Akademska misao, Belgrade, 2003, (in Serbian).

[10] J. G. Proakis, *Digital Communications,* McGraw-Hill. New York, 2000.

[11] M. D. Yacoub, "The α-μ distribution: a general fading distribution," *in Proc. IEEE Inter. Symp. on Personal, Indoor and Mobile Radio Commun.,* vol. 2, pp. 629-633, Sept. 2002.

[12] M. D. Yacoub, "The α-μ distribution: a physical fading model for the Stacy distribution," *in IEEE Trans. Veh. Technol.,* vol. 56, no. 1, pp. 27-34, Jan. 2007.

[13] V. A. Aalo, T. Piboongungon, and C.-D. Iskander, "Bit-error rate of binary digital modulation schemes in generalized Gamma fading channels," *IEEE Common. Lett.,* vol.9, no.2, pp. 139-141, Feb. 2005.

[14] T. Piboongungon, V. A. Aalo, and C.-D. Iskander, "Average error rate of linear diversity reception schemes over generalized gamma fading channels*," in* Proc. IEEE Southeastcon*, Ft. Lauderdale, FL,* Apr. 2005. pp 265-270.

[15] W. C. Lindsey, M. K. Simon, *Telecommunication Systems Engineering.* Prentice-Hall, Inc., Englewood Clifs, NJ, 1973.

[16] I. S. Gradsteyn, I. M. Ryzhik, *Table of Integrals, Series, and Products.* 6th ed., New York: Academic, 2000.

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Multivariable Modeling and Decentralized Robust Linear Controllers for Current-Sharing DC/DC Converters

Aleksandar Ž. Rakić, Trajko B. Petrović

Abstract—In this paper, the multivariable approach is utilized to obtain linear models of current-sharing switching converters. These multivariable linear models are suited for frequency framework of various linear control design techniques. Frequency domain setup is proposed for the robust linear design and all of its elements are defined in order to obtain simple decentralized robust PI/PID type controllers by reduction. The feasibility of the approach is verified for robustness and performance in a three parallel boost converters case study.

Index Terms—modeling, robust control, DC/DC converters, current sharing.

I. INTRODUCTION

HIGH power demands of the consumer electronics, modularity and redundancy requirements often bring out the need of several switching power supplies [1, 2] working in parallel and sharing the current to be supplied to the load.

Linear controllers are dominant and wide accepted for their simplicity, common understanding and clear insight to control design impact on fulfillment of stability and performance requirements.

On the other hand, in current-sharing applications there exists abundance of feedback loops which make problem multivariable i.e. hard for modeling, analysis and control design. Also, linear controllers usually suffer of weak performance or even instability when large scale disturbance or significant set point changes are applied. The idea to overcome the drawbacks of the linear approach to the control design is to derive the appropriate multivariable model of the current-sharing configuration, suitable for the multivariable robust control design.

Multivariable robust linear control design [3-5] will make the system insensitive to the uncertainties of modeling and its industry application is getting wider acceptance nowadays for powerful support in research and development phase of the design, like [6] and [7].

Further fuzzification, resulting in robust fuzzy control, is perspective to improve large signal responses [8].

The purpose of this paper is to utilize the multivariable approach in order to obtain linear models of current-sharing switching converters as the alternative to simplified conventional linear approach to modeling [9-14]. Obtained multivariable linear models are to be suitable for frequency framework of various linear control design techniques and they will be used to obtain robust, but simple PI/PID controllers, applicable according to industrial needs.

The paper is organized in sections. Sect. 2 is the place where the existing multivariable model [15] is presented. The subject of Sect. 3 is the derivation of the proposed full multivariable state-space model. In Sect. 4 the proper framework for the robust linear control design is introduced and discussed. Sect. 5 consists of the control design verification in the case study. The conclusion is presented in Sect. 6.

II. PARALLELING SINGLE UNIT LINEAR MODELS

The power stage of each converter (like the boost given for example in Fig. 1) is a variable structure process, depending on the state of the control switch Q within the switching period:

- while $nT \leq t \leq nT+t_{on}$, switch in ON, structure is S1,
- while $nT+t_{on} \leq t \leq (n+1)T$, switch is OFF, structure is S2.

Introducing: duty ratio $d_{Qn} = t_{on} / T$, state variables $\mathbf{x} = [v_C \quad i_L]^T$ and external inputs $\mathbf{d} = [v_{IN} \quad i_G]^T$, the state space models become:

$$\dot{\mathbf{x}}(t) = A_1\mathbf{x}(t) + E_1\mathbf{d}(t), \ nT < t < (n+d_{Qn})T , \qquad (1)$$

$$\dot{\mathbf{x}}(t) = A_2\mathbf{x}(t) + E_2\mathbf{d}(t), \ (n+d_{Qn})T \leq t < (n+1)T . \qquad (2)$$

State-space averaging gives nonlinear model:

$$\dot{\mathbf{x}}(t) = A\mathbf{x}(t) + E\mathbf{d}(t),$$
$$A = d_{Qn}A_1 + (1-d_{Qn})A_2, \quad E = d_{Qn}E_1 + (1-d_{Qn})E_2 \qquad (3)$$

The control signal, the input signals, the states, and the output signals can be divided into the stationary values and the increments:

$$d_Q = D_Q + d_q, \ \mathbf{d} = \mathbf{D} + \hat{\mathbf{d}}, \ \mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}, \ \mathbf{y} = [v_{OUT} \quad i_L]^T = \mathbf{Y} + \hat{\mathbf{y}}. \ (4)$$
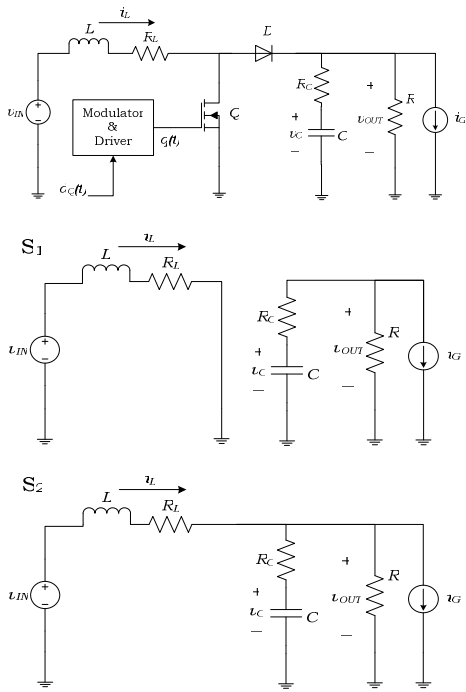
Fig. 1. Boost power stage (top), Switching structure S1 (middle), Switching structure S2 (bottom).

$$\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}, \ \mathbf{y} = \begin{bmatrix} v_{OUT} & i_L \end{bmatrix}^T = \mathbf{Y} + \hat{\mathbf{y}}. \tag{5}$$

Assuming the increments are small enough:

$$\left\| D_Q \right\| \gg \left\| d_q \right\|, \ \ \left\| \mathbf{D} \right\| \gg \left\| \hat{\mathbf{d}} \right\|, \ \ \left\| \mathbf{X} \right\| \gg \left\| \hat{\mathbf{x}} \right\|, \ \ \left\| \mathbf{Y} \right\| \gg \left\| \hat{\mathbf{y}} \right\|, \tag{6}$$

$$\hat{\mathbf{x}} = \begin{bmatrix} v_c & i_L \end{bmatrix}^T, \ \hat{\mathbf{y}} = \begin{bmatrix} v_{out} & i_L \end{bmatrix}^T, \ \hat{\mathbf{d}} = \begin{bmatrix} v_{in} & i_g \end{bmatrix}^T, \tag{7}$$

linearization of the averaged nonlinear model gives the Single Unit Linear (SUL) model:

$$\dot{\hat{\mathbf{x}}} = A\hat{\mathbf{x}} + B d_q + E\hat{\mathbf{d}}, \ \hat{\mathbf{y}} = C\hat{\mathbf{x}} + D d_q + F\hat{\mathbf{d}}, \tag{8}$$

where the state-space matrices are given by:

$$A = A_1 D_Q + A_2 (1 - D_Q), \quad B = (A_1 - A_2)\mathbf{X} + (E_1 - E_2)\mathbf{D},$$
$$C = C_1 D_Q + C_2 (1 - D_Q), \quad D = (C_1 - C_2)\mathbf{X} + (F_1 - F_2)\mathbf{D}, \tag{9}$$
$$E = E_1 D_Q + E_2 (1 - D_Q), \quad F = F_1 D_Q + F_2 (1 - D_Q).$$

Relevant transfer function matrices in the small signal input-output representation of the process:

$$\hat{\mathbf{y}} = \begin{bmatrix} v_{out}(s) \\ i_L(s) \end{bmatrix} = \underbrace{\begin{bmatrix} P_v(s) \\ P_i(s) \end{bmatrix}}_{\tilde{P}(s)} d_q(s) + \underbrace{\begin{bmatrix} A_s(s) & Z_{out}(s) \\ Y_{in}(s) & T_c(s) \end{bmatrix}}_{\tilde{P}_d(s)} \underbrace{\begin{bmatrix} v_{in}(s) \\ i_g(s) \end{bmatrix}}_{\mathbf{d}(s)} \tag{10}$$

are defined by the state-space matrices in the following way:

- $\tilde{P}(s)$ has state-space representation (A, B, C, D),

- $\tilde{P}_d(s)$ has state-space representation (A, E, C, F),

where matrices A, B, C, D, E and F are given in (9).

Small signal model of the overall process of current-sharing power stages is given by the equations:

$$v_{out} = \frac{1}{1/R_{load} + \sum_{j=1}^{n} 1/Z_{out\,j}} \left(\sum_{j=1}^{n} \left(\frac{P_{v\,j} d_{q\,j} + A_{s\,j} v_{in}}{Z_{out\,j}} \right) + i_g \right) \tag{11}$$

$$i_{L\,j} = P_{i\,j} d_{q\,j} + Y_{in\,j} v_{in} + \frac{1}{\frac{1}{R_{load}} + \sum_{j=1}^{n} \frac{1}{Z_{out\,j}}} \cdot \frac{T_{c\,j}}{Z_{out\,j}} i_g, \ j = 1,..,n \tag{12}$$

where: R_{load} is the nominal load, $P_{v\,j}$, $P_{i\,j}$, $A_{s\,j}$, $Y_{in\,j}$, $T_{c\,j}$ and $Z_{out\,j}$ are: transfer function from control to the output voltage, transfer function from control to the unit's current, audio susceptibility, input admittance, transcoductance and output impedance, all for the j-th unit, respectively.

Introducing the vectors of the input, the disturbance and the output:

$$\mathbf{u} = [d_{q1} \ d_{q2} \ ... \ d_{qn}]^T, \ \mathbf{d} = [v_{in} \ i_g]^T, \ \mathbf{y} = [v_{out} \ i_{L1} \ ... \ i_{Ln}]^T, \tag{13}$$

Paralleled Single Unit Linear (PSUL) model can be presented in the matrix form:

$$\mathbf{y} = \mathbf{P}_1 \mathbf{u} + \mathbf{P}_2 \mathbf{d}, \tag{14}$$

which involve transfer function matrices:

$$\mathbf{P}_1 = \begin{bmatrix} P'_{v1} & \cdots & P'_{vn} \\ P_{i1} & 0 & 0 \\ 0 & \ddots & 0 \\ 0 & 0 & P_{in} \end{bmatrix}, \ \mathbf{P}_2 = \begin{bmatrix} \sum_{j=1}^{n} A'_{sj} & Z'_{out} \\ Y_{in1} & T'_{c1} \\ \vdots & \vdots \\ Y_{in\,n} & T'_{cn} \end{bmatrix} \tag{15}$$

with the constituting transfer functions:

$$Z'_{out} = \frac{1}{\frac{1}{R_{load}} + \sum_{j=1}^{n} \frac{1}{Z_{out\,j}}}, \ P'_{v\,j} = \frac{Z'_{out}}{Z_{out\,j}} P_{v\,j},$$

$$A'_{s\,j} = \frac{Z'_{out}}{Z_{out\,j}} A_{s\,j}, \ T'_{c\,j} = \frac{Z'_{out}}{Z_{out\,j}} T_{c\,j}. \tag{16}$$

III. FULL MULTIVARIABLE STATE SPACE MODEL

Introducing the full state vector of the current-sharing configuration:

$$\mathbf{x} = [v_{C1} \ ... \ v_{Cn} \ i_{L1} \ ... \ i_{Ln}]^T, \tag{17}$$

and using the disturbance vector $\mathbf{d}$ defined in (13), Kirchoff's laws for the overall system can be arranged in the form:

$$\dot{\mathbf{x}} = A_0 \mathbf{x} + E_0 \mathbf{d}$$
$$+ A_{1j} \mathbf{x} + E_{1j} \mathbf{d} + A_{2j} \mathbf{x} + E_{2j} \mathbf{d} \ (direct\,control\,term) \tag{18}$$
$$+ A_{1k} \mathbf{x} + E_{1k} \mathbf{d} + A_{2k} \mathbf{x} + E_{2k} \mathbf{d} \ (indirect\,control\,term),$$

where the indexing terms consist of: "j" – direct influence of j-th switch control to the j-th capacitance voltage and j-th inductor current, "k" – indirect influence of k-th switch control to the j-th capacitance voltage and j-th inductor current, "1" – influence when switch in ON, "2" – influence when switch in OFF and "0" – influence not altered by the position of switches.

In the similar manner, output equations can be arranged in the form:

$$\mathbf{y} = C_0 \mathbf{x} + F_0 \mathbf{d} + C_{1j} \mathbf{x} + F_{1j} \mathbf{d} + C_{2j} \mathbf{x} + F_{2j} \mathbf{d}, \tag{19}$$

where the output vector $\mathbf{y}$ in given in (13).

Multi-input state-space averaging and linearization give Full Multivariable State Space Linear (FMSSL) model:

$$\dot{\mathbf{x}} = A\hat{\mathbf{x}} + Bd_q + E\hat{\mathbf{d}}, \quad \hat{\mathbf{y}} = C\hat{\mathbf{x}} + Dd_q + F\hat{\mathbf{d}}, \tag{20}$$

where the state space matrices are:

$$A = A_0 + \left(A_{1j} + A_{1k} \right) D_Q + \left(A_{2j} + A_{2k} \right)(1 - D_Q),$$

$$E = E_0 + \left(E_{1j} + E_{1k} \right) D_Q + \left(E_{2j} + E_{2k} \right)(1 - D_Q),$$

$$B_j = (A_{1j} - A_{2j})\mathbf{X} + (E_{1j} - E_{2j})\mathbf{D},$$

$$B_k = (A_{1k} - A_{2k})\mathbf{X} + (E_{1k} - E_{2k})\mathbf{D}, \tag{21}$$

$$B = diag(B_j) + offdiag(B_k),$$

$$C = C_0 + C_{1j}D_Q + C_{2j}(1 - D_Q),$$

$$F = F_0 + F_{1j}D_Q + F_{2j}(1 - D_Q),$$

$$D_j = (C_{1j} - C_{2j})\mathbf{X} + (F_{1j} - F_{2j})\mathbf{D}, \quad D = diag(D_j).$$

For the purposes of the comparison with PSUL and the notation in the control framework, transfer function matrix representation of FMSSL model is given also in the form of (14), where:

- $\mathbf{P}_1(s)$ has state-space representation (A, B, C, D),
- $\mathbf{P}_2(s)$ has state-space representation (A, E, C, F),

and matrices A, B, C, D, E and F are given in (21).

IV. FREQUENCY DOMAIN FRAMEWORK FOR THE ROBUST LINEAR DESIGN

Since the output vector $\mathbf{y}$ is of dimension $n+1$ and there are only n independent input switch control signals, the transfer function matrix $\mathbf{P}_1$ is not square. One way to make it square, in order to obtain a closed-loop control, is to redefine the outputs to represent the output voltage and the current distribution between the units [12]:

$$\mathbf{y}' = \begin{bmatrix} v_{out} & \Delta i_{L2} & \Delta i_{L3} & \cdots & \Delta i_{Ln} \end{bmatrix}^T, \quad \Delta i_{Li} = i_{Li} - i_{L1}. \tag{22}$$

The transformation matrix:

$$\mathbf{S} = \begin{bmatrix} 1 & 0 & 0 & 0 & \cdots & 0 \\ 0 & -1 & 1 & 0 & \cdots & 0 \\ 0 & -1 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & 0 \\ 0 & -1 & 0 & 0 & 0 & 1 \end{bmatrix}_{n \times (n+1)} \tag{23}$$

introduces the current difference between the i-th unit and the reference (master) unit 1, making the squared plant $\mathbf{S} \cdot \mathbf{P}_1$ suitable for control. Moreover, *master-slave* (M-S) control configuration can be represented by matrix equation:

$$\mathbf{u} = \mathbf{S}_c \mathbf{K} \mathbf{e}, \quad \mathbf{K} = diag(K_v, K_{i2}, ..., K_{in}), \tag{24}$$

where: error vector $\mathbf{e}$ is the input to controller $\mathbf{K}$, and the introduced matrix

$$\mathbf{S}_c = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ 1 & 1 & 0 & \cdots & 0 \\ 1 & 0 & 1 & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & 0 \\ 1 & 0 & \cdots & 0 & 1 \end{bmatrix}_{n \times n} \tag{25}$$

make generalized plant:

$$\mathbf{P}_g = \mathbf{S} \mathbf{P}_1 \mathbf{S}_c \tag{26}$$

suitable for decoupled consideration of voltage and current control. Namely, first channel of $\mathbf{P}_g$ corresponds to the nominal plant for the voltage control:

$$G_v(s) = \mathbf{P}_g(1,1), \tag{27}$$

and all the other diagonal channels represent nominal plants for the control of the current loops:

$$G_i(s) = \mathbf{P}_g(i,i), \quad i \neq 1. \tag{28}$$

The block diagram of the robust linear (RL) control design setup is presented in Fig. 2, with following signals denoted: r – the reference (set-point) signal, d – the disturbance signal, $e = r - y$ is the error in reference tracking, e' – the performance weighted error, and u – the control signal. Relevant transfer functions are: $G(s)$ – the nominal linear model of the plant, $G_d(s)$ – the disturbance model, $K(s)$ – the linear robust controller to be designed, $W_i(s)$ – the multiplicative input uncertainty bound (uncertainty weighting function), $\boldsymbol{\Delta}(s)$ – an unknown but unity-normed multiplicative uncertainty of modeling, and $W_p(s)$ – the performance weighting function.
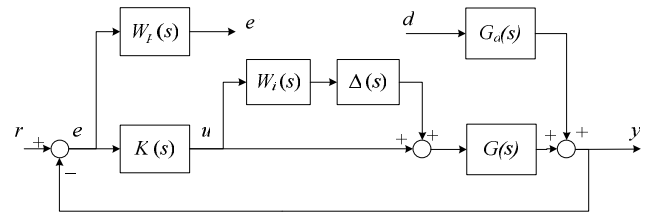
Fig. 2. Block Diagram of Robust Linear (RL) Control Setup.

RL control setup is to be used twice in M-S control design: once for the synthesis of the voltage controller, and the other time for the synthesis of the current controller. All the converter modules are assumed to be identical.

For the design of the voltage controller $K(s) = K_v(s)$, suitable models of the plant and disturbance are:

$$G(s) = G_v(s), \quad d = i_g, \quad G_d(s) = Z_{out}(s), \tag{29}$$

while for the current control $K(s) = K_i(s)$, suitable choice is:

$$G(s) = G_i(s) = P_i(s), \quad d = 0, \text{ reference tracking.} \tag{30}$$

The parameters of the frequency domain control design are the weighting functions mentioned above. They are adopted in the following form:

$$W_p(s) = \frac{1}{M_S^*} \frac{s + M_S^* \omega_0^*}{s + A \omega_0^*}, \tag{31}$$

$$W_i(s) = MIU^* \frac{s/\omega_{0T}^* + 1}{s/(B\omega_{0T}^*) + 1}. \tag{32}$$

The meaning of the parameters in (31) – (32) and recommended choices are given in Table 1.

The only parameter to tune in the proposed design *is the bandwidth ω_0^** of the closed loop control, while the other parameters are chosen to fit the wide range of plants and their change is rarely needed (and has small impact on control design). For the reference tracking, minimization:

$$\gamma_{rt\,\mu/\infty} = \min_{K(s)} \left\| \begin{matrix} W_p S G_d \\ W_i T \end{matrix} \right\|_{\mu/\infty} = \min_{K(s)} \left\| \begin{matrix} W_p (1+GK)^{-1} G_d \\ W_i GK(1+GK)^{-1} \end{matrix} \right\|_{\mu/\infty} \quad (33)$$

is carried out, while for the disturbance rejection adequate minimization is:

$$\gamma_{dr\,\mu/\infty} = \min_{K(s)} \left\| \begin{matrix} W_p S \\ W_i T \end{matrix} \right\|_{\mu/\infty} = \min_{K(s)} \left\| \begin{matrix} W_p (1+GK)^{-1} \\ W_i GK(1+GK)^{-1} \end{matrix} \right\|_{\mu/\infty}. \quad (34)$$

The choice of performance weighting function W_p forces the μ/H_∞ controller to be in the form of causal PI proportional-integral (PI) or causal proportional-integral-derivative (PID) controller, plus the higher order dynamics. When the control design is obtained, zero-pole cancellation should be applied and dynamics much higher then bandwidth should be neglected, so the final reduced robust linear controllers will be in the form of causal PI:

$$K_{PI}^{RL}(s) = \frac{K_0 (s/\omega_z + 1)}{s(s/\omega_p + 1)} \quad (35)$$

or causal PID:

$$K_{PI}^{RL}(s) = \frac{K_0 (s^2/\omega_z^2 + 2\zeta s/\omega_z + 1)}{s(s/\omega_p + 1)}, \quad (36)$$

where K_0 is the velocity constant of the controller and the parameters ω_z and ω_p are natural frequencies of the controller's zero and pole.

V. CASE STUDY VERIFICATION OF THE PROPOSED DESIGN

In order to verify the proposed design, three boost converters working in parallel will be considered with the following parameters: f_{sw} = 200kHz, V_{IN} = 18V, V_{OUT} = 25V, R_{load} = 4.17Ω, L = 41.67μH, $R_L \approx$ 50mΩ, C = 26.67μF, $R_C \approx$ 25mΩ. Due to space limitation, the state space matrices of PSUL and FMSSL models of the case study plant are omitted.

In Fig. 3, PSUL and FMSSL models are compared for small signal transfer functions from the j-th control to the outputs: the regulated voltage v_{out} and the j-th inductor current. Significant differences are found in the high frequency region and they are presumed to be the result of the PSUL's neglected

TABLE I
PARAMETERS OF LINEAR ROBUST CONTROL DESIGN

Param.	Description	Recommended Value
ω_0^*	Closed-Loop Bandwidth	According to process open-loop characteristics
M_S^*	Maximum Sensitivity	1.2
MIU^*	Bound of Multiplicative Input Uncertainty	0.8
ω_{0T}^*	Bandwidth of Modeling Certainty	the same value as chosen ω_0^*
A	Sensitivity Function Low Frequency Gain (introduced for numerics)	10^{-4} (-80dB)
B	Multiplicative Constant for W_i Pole Placement (introduced for numerics)	10

multivariable dynamics. This conclusion is supported by the comparison in Fig. 4 of the FMSSL's transfer functions with the same ones obtained in Spice with the Voltage Mode Large Signal Continuous Conduction Mode (VMLSCCM) model of the switches. The gain of the FMSSL is the good model of the multivariable interconnection i.e. the transfer function from the k-th control to the j-th inductor current (Fig 4. bottom), fully neglected in PSUL modeling. In Fig. 5, FMSSL's disturbance transfer functions are also found to fit the behavior of the realistic Spice model. Therefore, the following controller design will be based exclusively on the FMSSL model.

The bandwidths of the robust linear controllers are adopted to be: 5 kHz for the voltage loop and 20 kHz for the current loop. Obtained μ/H_∞ controllers are reduced to:

$$K_{vPID}^{RL}(s) = \frac{515.8\left(s^2/(1.373 \cdot 10^4)^2 + s/(1.14 \cdot 10^4) + 1\right)}{s\left(s/(2.854 \cdot 10^5) + 1\right)}. \quad (37)$$

$$K_{iPI}^{RL}(s) = \frac{227.5(s/1330 + 1)}{s\left(s/(4.59 \cdot 10^5) + 1\right)} \quad (38)$$

The verification of the control design large is conducted through simulation [6].
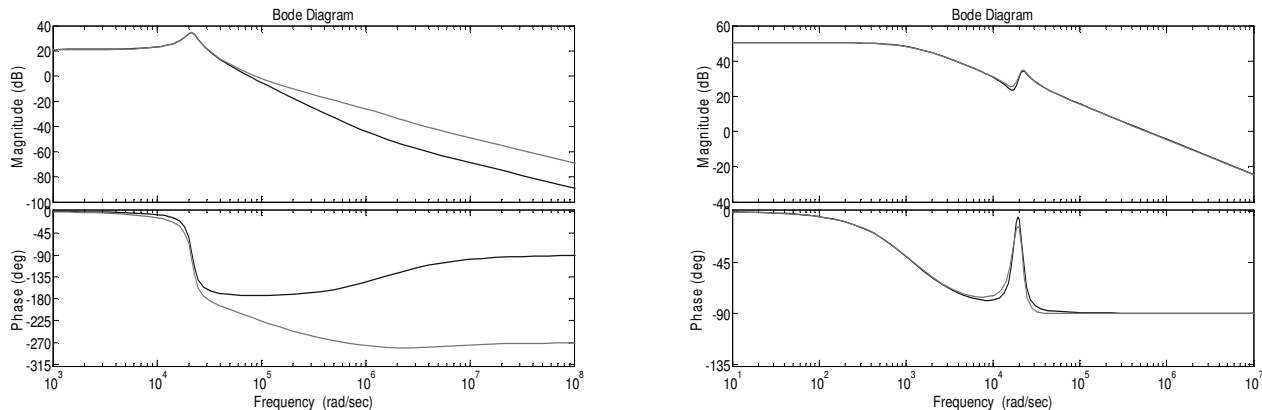
Fig. 3. Small signal transfer functions: left – from control to the output voltage, right –from control q_j to inductor current i_{Lj} (PSUL – black, FMSSL – gray).
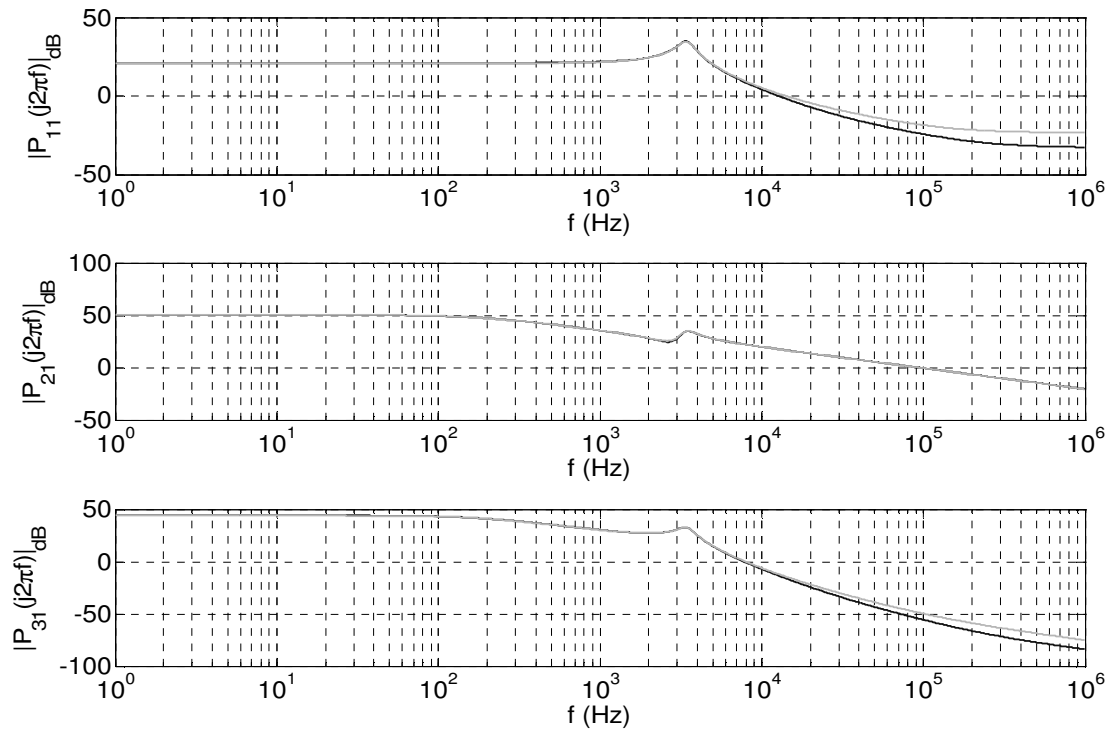
Fig. 4. Small signal transfer functions: top – from control to the output voltage, middle – from control q_j to inductor current i_{Lj}, bottom – from control q_k to inductor current i_{Lj}, (Spice VMLSCCM – black, FMSSL – gray).
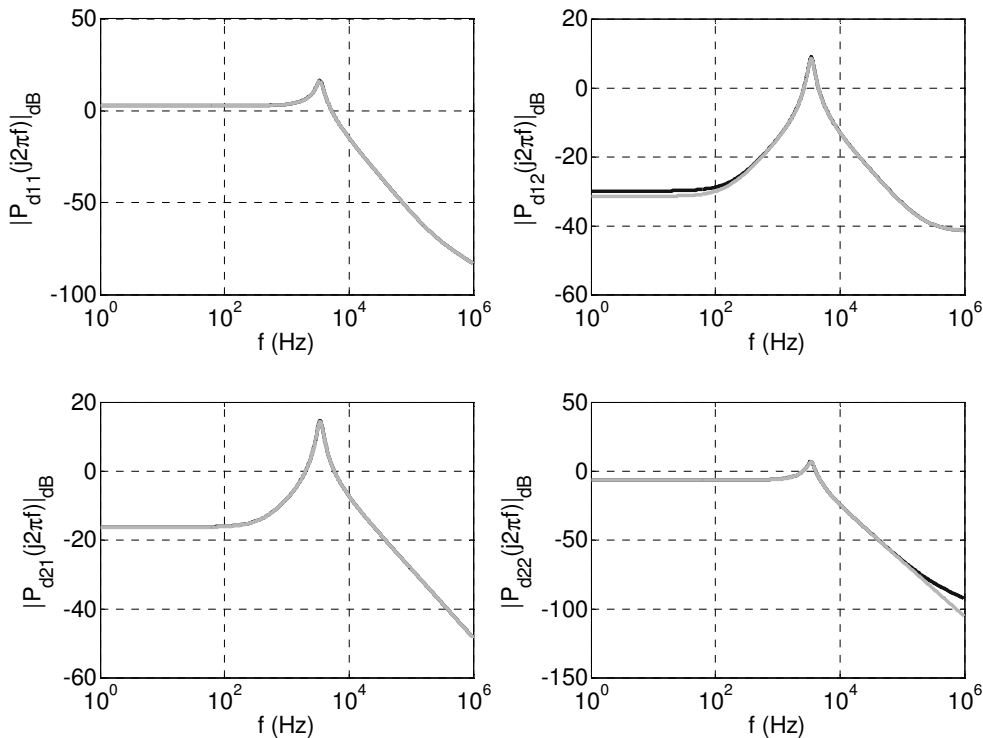
Fig. 5. Small signal transfer function matrix from the disturbance vector to the output voltage and one of the inductor currents (Spice VMLSCCM – black, FMSSL – gray).

In order to test robustness of the control to the tolerance of the components, the parameters of the units in a three boost setup are perturbed in the following way:

- the gain of the voltage loop is increased by 20%,
- control-to-current gain of unit #2 is increased by 20% ,
- control-to-current gain the unit #3 is decreased by 20%.

The first experiment was the load change step from full load to 50% (from 3×2A to 3×1A) and the unit currents along with voltage waveform and the control signals (duty ratios) are presented in Fig. 6. No significant deterioration of the perturbed plant case comparing to nominal is observed.
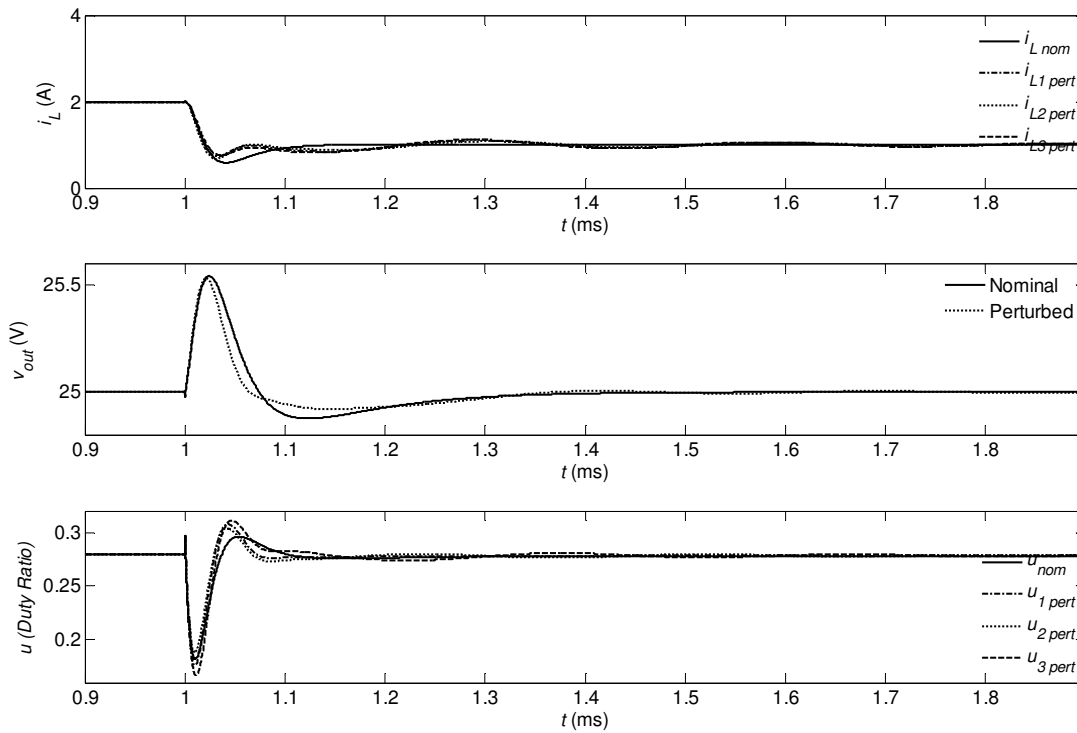
Fig. 6. Responses to Load Step from Full Current Load to 50% Load.
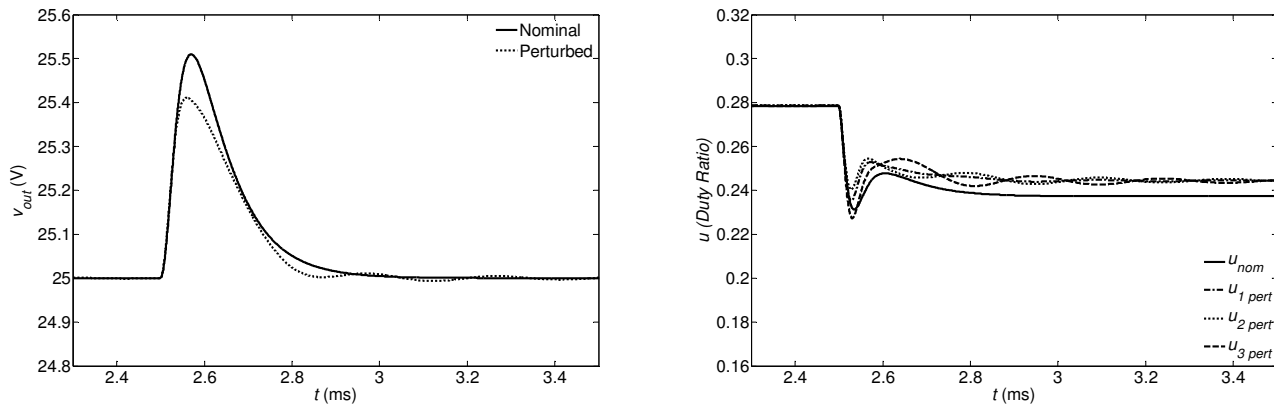
Fig. 7. Responses to Supply Voltage Deviation Step in Amount of 1V.

The second experiment was the voltage supply step change in amount of $v_{in} = 1V$, where the open-loop voltage drop effect would be approx. $v_{in}/(1-d_Q) \approx 1.39V$. It can be seen in Fig. 7, as well as in the previous experiment, disturbance is eliminated in the short time and with the desirable waveforms and amplitudes of the control signals.

VI. CONCLUSION

In this paper, multivariable modeling approach is utilized to obtain new linear state-space model of the current-sharing converters.

Benefits of the proposed FMSSL are in the field of interactions in the multivariable plant of current-sharing converters, neglected in existing PSUL model. FMSSL shows good agreement with the small signal multivariable behavior obtained by the Spice model.

Proposed FMSSL model is derived in the state-space, so it is the minimal realization. As such, it is suitable for the various control designs resulting in controllers of minimal order.

As a perspective candidate for maximization of robustness and performance, robust control design is carried out and optimal robust linear controllers are obtained and they are reduced to simple decentralized PI and PID type controllers. Proposed robust design is successfully verified in the case study with three paralleled boost converters.

Further research will be directed towards the analysis of the FMSSL robustness properties (uncertainty bounds), application of the proposed model in the appropriate control designs and extension of the proposed multivariable approach to the random switching schemes for electromagnetic emission reduction in distributed current-sharing applications.

REFERENCES

[1] N. Mohan et al., *Power Electronics.* NY-USA: John Willey, 1995.

[2] D. M. Mitchell, *DC/DC Switching Regulator Analysis.* NY-USA: McGraw-Hill, 1988.

[3] S. Skogestad, and I. Postlethwaite, *Multivariable Feedback Control.* England: John Willey & Sons, 1996.

[4] M. Morari, and E. Zafiriou, *Robust Process Control.* NY-USA: Prentice Hall, 1989.

[5] K. Zhou et al. *Robust and Optimal Control.* NJ-USA: Prentice Hall, 1996.

[6] *Matlab & Simulink.* The MathWorks Inc, MA-USA, 2008.

[7] *MatrixX: Xmath & SystemBuild*, National Instruments, TX-USA, 2004.

[8] A. Ž. Rakić, T. B. Petrović, D. M. Dujković, "Systematic Approach to Robust Fuzzy Control Design for Master-Slave Current-Sharing DC/DC Converters, in *INDEL '06 Conf.*, Banja Luka, Republic of Srpska – Bosnia and Herzegovina, 2006, pp. 269–274.

[9] L. R. Lewis, B. H. Cho, F. C. Lee, and B. A. Carpenter, "Modeling and analysis of distributed power systems," in *Proc. IEEE PESC'89*, 1989, pp. 152–159.

[10] B. Choi, B. H. Cho, R. B. Ridley, and F. C. Lee, "Control strategy for multi-module parallel converter systems," in *Conf. Rec. PESC'90*, 1990, pp. 225–234.

[11] K. Siri, C.Q. Lee, and T. F. Wu, "Current Distribution For Parallel Connected Converters: Part I", *IEEE Trans. Aerosp. Electron. Syst.,* vol. 28, pp. 829-840, July 1992.

[12] Y. Panov, J. Rajagopalan, and F. C. Lee, "Analysis and Control Design of N Paralleled DC-DC Converters with Master-Slave Current Sharing Control", Applied Power Electronics Conference '97 Proc., 1997, pp. 436-442.

[13] V. J. Thottuvelil, G. C. Verghese, "Analysis and Control Design of Paralleled DC/DC Converters with Current Sharing", *IEEE Trans. Power Electron.,* vol. 13, pp. 635-644, July 1998.

[14] B. Choi, "Comparative Study on Paralleling Schemes of Converter Modules for Distributed Power Applications", *IEEE Trans. Ind. Electron.,* vol. 45, pp. 194-199, Apr. 1998.

[15] Đ. S. Garabandić, and T. B. Petrović, "Modeling Parallel Operating PWM DC/DC Power Supplies", *IEEE Trans. Ind. Electron.*, vol. 42, pp. 545-551, Oct. 1995.

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Power Quality Monitoring and Power Measurements by Using Virtual Instrumentation

Z. Kokolanski, M. Srbinovska, A. Simevski, C. Gavrovski and V. Dimcev

Abstract—**The presented paper describes a virtual instrument used for monitoring and analysis of the relevant power quality parameters and power measurements.**

The metrological support block is realized in LabVIEW environment which uses advanced methods for measurement and recording of the power quality parameters in accordance with the European quality standards. In that way, a suitable hardware solution for signal conditioning and load control is proposed. The most important parameters (voltage, current, power) are recorded into text files which are further used for measurement data analyses. The measurement results are obtained by using waveform simulator METREL.

Index Terms—**Power Quality, Data Acquisition, Virtual Instrumentation.**

I. INTRODUCTION

THE electric power is essential for running industrial production processes, for commercial use, for transport and other purposes. In the last years this dependency has increased and all these processes relay on the quality of electricity supply, namely power quality [1]. The detection of the disturbances affecting the line voltages is one of the most qualifying points in the estimation of the "voltage quality" or "supply quality". The correct assessment of the quality of the supplied voltage has become one of the key issues in the deregulated electricity market. Ensuring a "high quality" of the supply voltage is the main requirement for ensuring a high "power quality".

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Great attention is therefore paid to the definition of suitable indexes of voltage quality and the definition of suitable measurement procedure to evaluate these indexes. A large number of power quality disturbances have been reported in the literature-some of them being transient in nature and others being related to periodic, steady – state operation. Some of the more common disturbances are: voltage and current harmonics [2,3], voltage dips, electric noise, impulses, notches and flicker.

Because of these disturbances measurement of the electric quantities, such as voltage, current and power by using equipment commonly used for measurement of sinusoidal signals can result in errors. In this way, inclusion of the digital signal processing techniques can be much more adequate. Anyway, a suitable digital signal processing approach must be provided.

In the recent years adoption of personal computers (PCs) in the field of the measurement technique offers great progress and flexibility. Step ahead for development of modern measurement systems is achieved by adopting the concept of Virtual Instrumentation. It is a methodology for realization of measurement instruments by using standard PC's, hardware data acquisition components for signal conversions and specialized program platforms for processing and recording of the measurement results.

In this paper a Virtual Instrument for power quality monitoring is proposed.

II. POWER QUALITY PARAMETERS

The ideal supply voltage is pure sinusoidal voltage with nominal frequency and nominal amplitude. Any variation from this is considered as a power quality event or a disturbance. One important aspect in the field of power quality is monitoring and control of the qualitative parameters of the electrical energy according to today's standards [4]. In that way, a big attention is paid to define the disturbances and determination of procedures for their measurement. A large number of power quality disturbances have been reported in the literature. In general, the parameters could be divided in two groups - voltage amplitude variations and wave-form distortion. A short classification of power quality parameters is given in Table I.

Variation of	Parameter
Frequency	Variation of power frequency
Voltage	Variation of magnitude of supplied voltage
	Rapid voltage changes
	Supply voltage dips and swells
	Voltage interruptions
	Flicker
Waveform	Supply voltage unbalance
	Transient overvoltages
	Voltage harmonics
	Voltage interharmonics
	Mains signaling voltage on the supply voltage
	Notching
	Noise

In the following section some theoretical analyses relied on the signal processing are reported.

III. SIGNAL PROCESSING ANALYZES

Analyzing a periodic signal $u(t)$ with angular frequency ω and having in mind the Nyquist criteria, the signal limited with it's Nth harmonic can be represented by $2N+1$ samples over the period T.

The active power value of the voltage $u(t)$ and current $i(t)$ is represented with the equation:

$$P = \frac{1}{T}\int_{0}^{T} u(t)i(t)dt \qquad (1)$$

Analyzing (1), measurement of the active power demands estimation of two time dependent components.

The p(t) spectrum is given by:

$$P(\omega) = U(\omega) * I(\omega) \qquad (2)$$

According to relation (2) the spectrum of $p(t)$ is wider than that of $u(t)$ and $i(t)$ and is limited to its $2N$th harmonic. From this analysis it can be clearly seen that if the moment value and the spectrum of the power is required, $u(t)$ and $i(t)$ must be sampled with frequency twice than the sampling theorem criteria. Theoretically, it is possible to acquire only $2N+1$ samples for the voltage and current, but in practice the sampling frequency must be significantly increased [5].

The same considerations can be applied for evaluation of the RMS value of $u(t)$ which is expressed by the relation:

$$U = \sqrt{\frac{1}{T}\int_{0}^{T} u^2(t)dt} \qquad (3)$$

The appropriate evaluation of (1) and (3) also demands for proper definition of the observation interval. The observation interval needs to be an integer multiply of the signal period T in order to minimize the leakage errors in the frequency domain. Otherwise under non-synchronous sampling conditions an interpolation algorithm must be employed.

IV. HARDWARE SOLUTION

The hardware is realized by using National Instruments multifunctional data acquisition (DAQ) card containing 32 analog input channels with resolution of 16 bits, programmable input range (±10V) and sampling rate up to 250kS/s. Two hardware boards for voltage and current signal conditioning are realized using six analog input channels, and three digital channels for load switching. The current measurement signals are obtained by using three electronic transducers incorporating current transformers and the load switching is realized by three relay switches controlled by the DAQ card. The voltage measurement signals from the power lines are obtained with precise resistive dividers. Block diagram of the hardware solution is shown in Fig.1
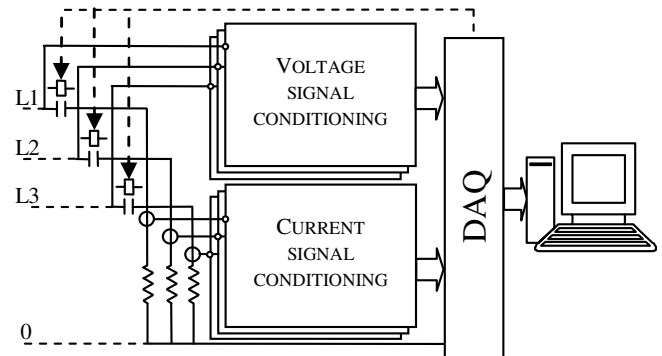
Fig. 1. Hardware block diagram

The signal conditioning circuits should provide few functions like: galvanic isolation from supply network, attenuation or amplification of the measured signals, protection of DAQ card and noise suppression. The main role of the signal conditioning circuit is to adjust the sensor's output signal span to match the analog-to-digital converter (ADC) input range.

The block diagram of the signal conditioning circuits is shown on Fig.2.
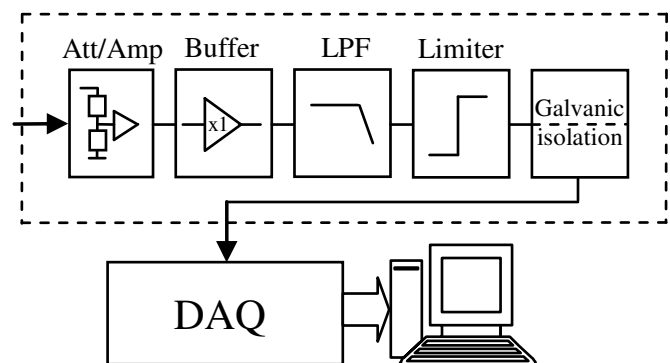
Fig. 2. Signal conditioning circuits block diagram

In the absence of proper signal conditioning the signal can exceed the ADC input range and cause saturation of its output. The signal is first attenuated or amplified and DC level shifted with the input attenuator/amplifier. The next block is a unity gain buffer with very high input impedance which is used for adaptation of the impedances of the attenuator and the filter. Sixth order active anti-aliasing filter has been designed with cut-off frequency of 6 kHz and near flat amplitude-frequency and phase-frequency characteristics. The filter is used before a signal sampler to restrict the signal's bandwidth and to satisfy the sampling theorem. Fast circuits for limiting the input voltage to the ADC input range have been designed. These circuits allow signals below a specified input level to pass unaffected while attenuating the peaks of stronger signals that exceed this level. The used data acquisition card is with galvanic isolated inputs. The galvanic separation eliminates all forms of operating disturbances such as ground loop and potential separation.

V. LabVIEW BASED Virtual Instrument

LabView is a National Instrument development software that allows rapidly and cost-effectively interface with measurement and control hardware, data analyzes, share results, and distribute systems. It is based on graphical programming techniques that allow programming with visual expressions, spatial arrangements of text and graphic symbols [6].

The software is based on a block diagram (intended for graphical program development) and front panel (graphic interface formed by switches and panels intended for user interaction).The Virtual Instrument described in this paper consists of two parts:
1) power line voltage analyzes
2) current and power analyzes

Fig.3 represents the voltage analyzes block diagram. This block is identical for all three power lines.
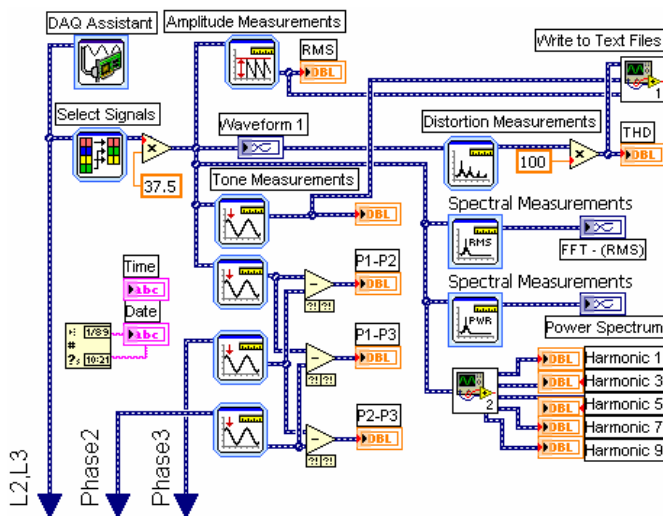
Fig. 3. Signal conditioning circuits block diagram

Samples from three analog channels are successively taken with sampling frequency of 2kHz per channel for sampling interval of 100ms and are fed to a signal selection block. Every sample is multiplied by a constant factor which indeed is the attenuation coefficient of the signal conditioning circuits. The obtained signal is further processed and used for measurement of the RMS, total harmonic distortion (THD), frequency and phase difference of the input signal.

The virtual instrument contains two sub-virtual blocks for filtration of the spectral components and data recording. The filtration block contains sixth order Chebyshev band pass IIR filters with central frequency at the odd spectral components and the data recording sub-virtual block stores the results for RMS, frequency and THD of the input signal in interval of 100ms.

The programming points are implemented as follows:
- Sample gathering;
- Voltage RMS calculation, equation (3);
- Frequency measurement;
- Phase difference calculation;
- Analyzes of the Total Harmonic Distortion, relation (4);

$$THD[\%] = \sqrt{\frac{\sum_{n} U_n^2}{U_1^2}} \cdot 100, n = 2,3..N \tag{4}$$

- Analyze amplitude spectrum by using Amplitude spectrum VI, equation (5);

$$AmplitudeSpectrum = \frac{FFT(\,signal\,)}{N} \tag{5}$$

- Analyze signal power spectrum using Auto Power spectrum VI, equation (6);

$$PowSpec = \frac{FFT^*(\,signal\,) \times FFT(\,signal\,)}{N^2} \tag{6}$$

where * is a complex conjugate.
- Display the signal waveform, amplitude and power spectrum on a waveform graph;
- Filtration and measurement of RMS for 5 odd spectral components;

For this purpose a sixth order Chebyshev band pass IIR filters are used with central frequency at the odd spectral components. The pass band of the filters is 20Hz.
- Write the amplitude RMS, signal frequency and THD into text files;

All measurement data with time and date of recording are recorded into separate text files. These data can be further used for data storage and analysis by using some graphical presentation software such as DIAdem or MS Excel.

Fig.4 represents the front panel of the virtual instrument
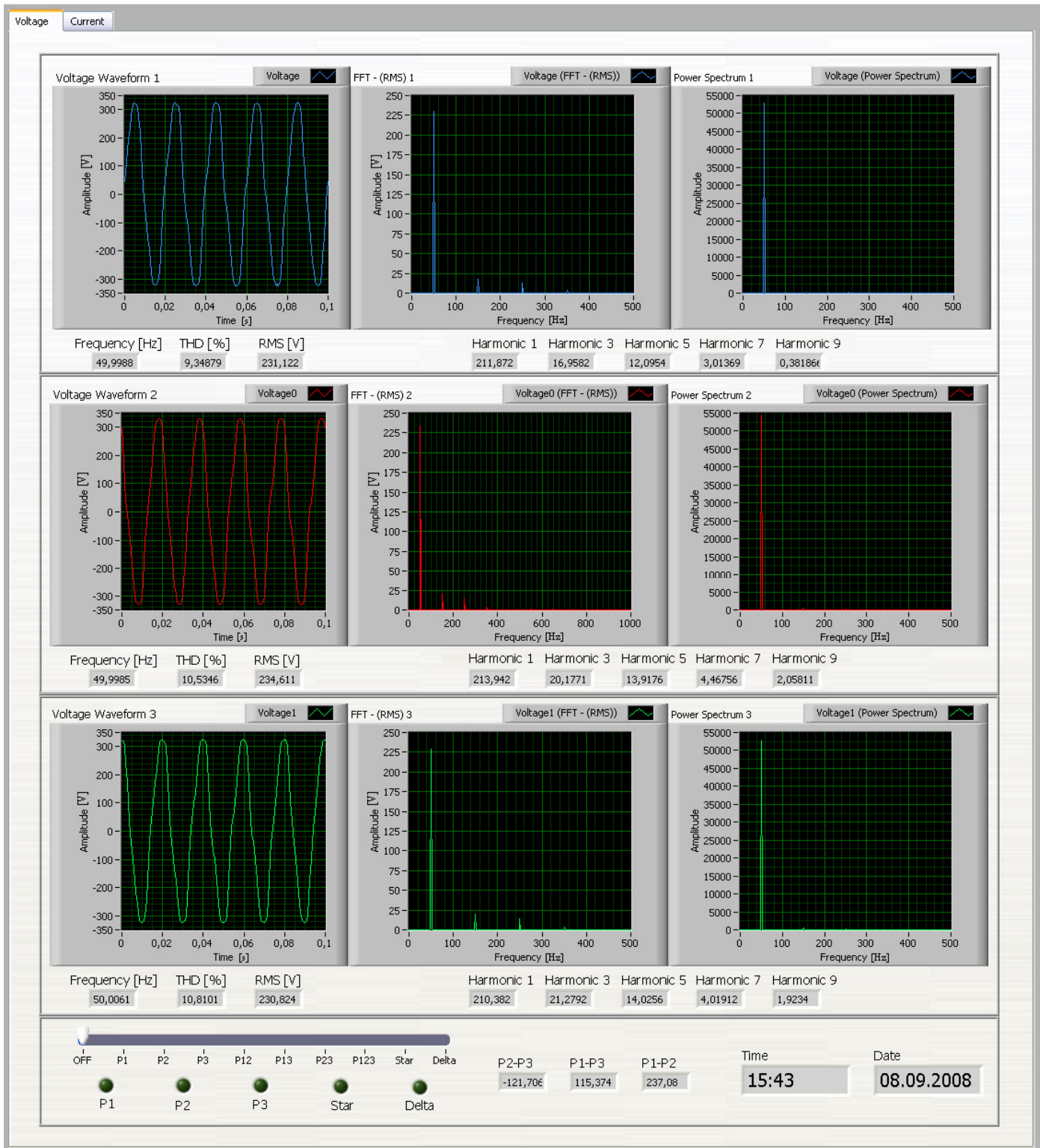
Fig. 4. Front panel of the virtual instrument

VI. CURRENT AND POWER ANALYZES

Three current channels are sampled with frequency of 2kHz per channel and a sampling interval of 100ms. Every sample is multiplied by constant factor corresponding to the transducer attenuation. The obtained signal is further processed and used for measurement of the RMS, total harmonic distortion (THD), and the active and reactive power of the input signal [7].

Fig.5 shows the LabView programming block diagram for current and power measurements for one measurement channel.
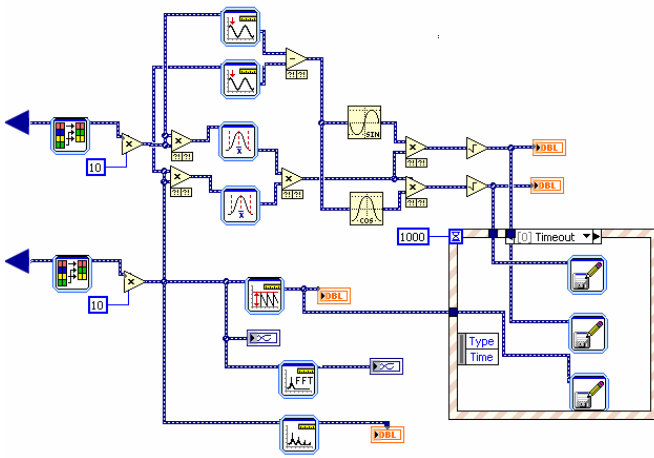
Fig. 5. Current and power measurements block diagram

The programming points are implemented as follows:
- Sample gathering;
- Current RMS calculation;
- Analyzes of the Total Harmonic Distortion;

- Analyze amplitude spectrum;
- Current phase measurement and current-voltage phase difference calculation;
- Active (7) and reactive (8) power calculation;

$$P = \sqrt{\sum_{i=0}^{N} U_i^2 \cdot \sum_{i=0}^{N} I_i^2 \, cos^2 \, \varphi_i} \qquad (7)$$

$$Q = \sqrt{\sum_{i=0}^{N} U_i^2 \cdot \sum_{i=0}^{N} I_i^2 \, sin^2 \, \varphi_i} \qquad (8)$$

- Display the signal waveform and amplitude spectrum on a waveform graph;
- Write the current RMS, active and reactive power into a text file;

The front panel corresponding to the LabView programming sequence is shown in (in) Fig.6
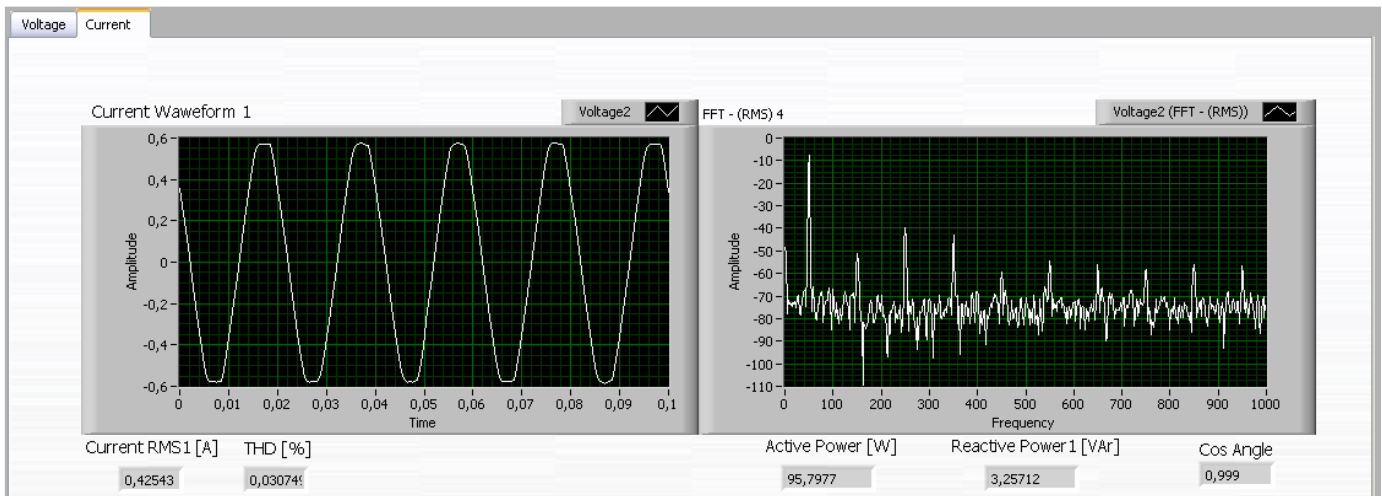
Fig. 6. Front panel of the virtual instrument for current and power measurements

VII. MEASUREMENT RESULTS

Measurement of the power quality is usually defined as a measurement of low frequency conducted disturbance with the addition of transient phenomena. The ideal single phase supply voltage is a pure sine wave with nominal frequency and voltage amplitude. Any variation of this is considered as a power quality disturbance.

The following parameters of supply voltage are influenced by disturbances:
- Frequency
- Voltage level
- Wave shape
- Symmetry of three phase system

In the experimental tests one phase power simulator Metrel MI 2191 is used [8]. The instrument is able to simulate typical voltage and current shapes, such as voltage

and current harmonics [2], flickers[9], transients[10], voltage interruptions [9] etc. Three examples for measurement of transients, flickers and harmonics are shown in the results.
- Transient is a term for short, highly damped momentary voltage or current disturbance Fig.7 and Fig.8;
- Flicker is a visual sense caused by unsteadiness of a light. The level of the sense depends on the frequency and magnitude of a light change and the observer itself Fig.9;
- Harmonics [3,4] are any periodic deviation of a pure sinusoidal voltage Fig.10;

Fig.11.a, Fig.11.b and Fig.11.c represent the recorded values for the RMS voltage, frequency and THD during 10 hour interval by using the text files from the virtual instrument. In the second experiment measurement of current and power of a 100W light is presented (Fig.6). Switching of the light is controlled by the DAQ card.
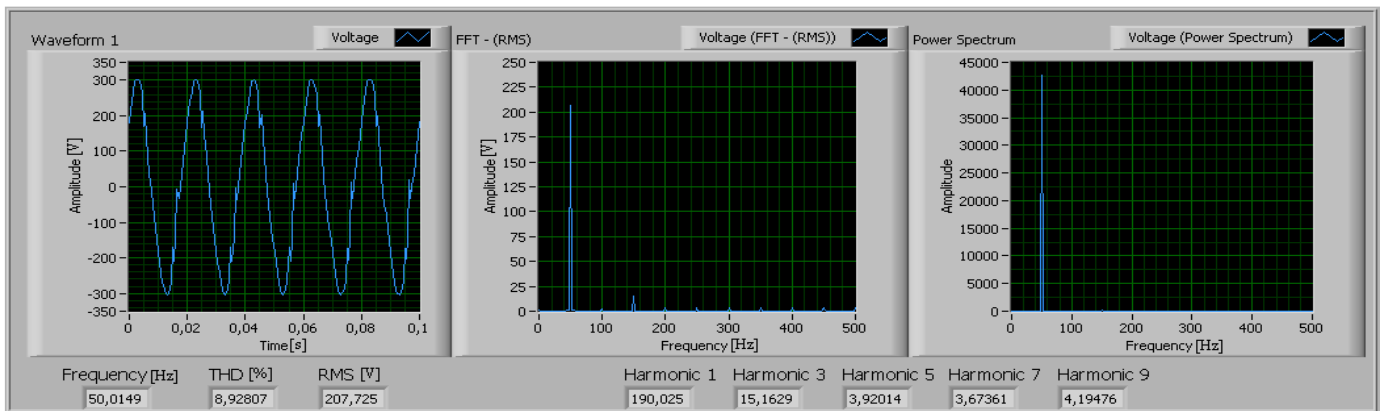
Fig. 7. Transients caused by SRC switching
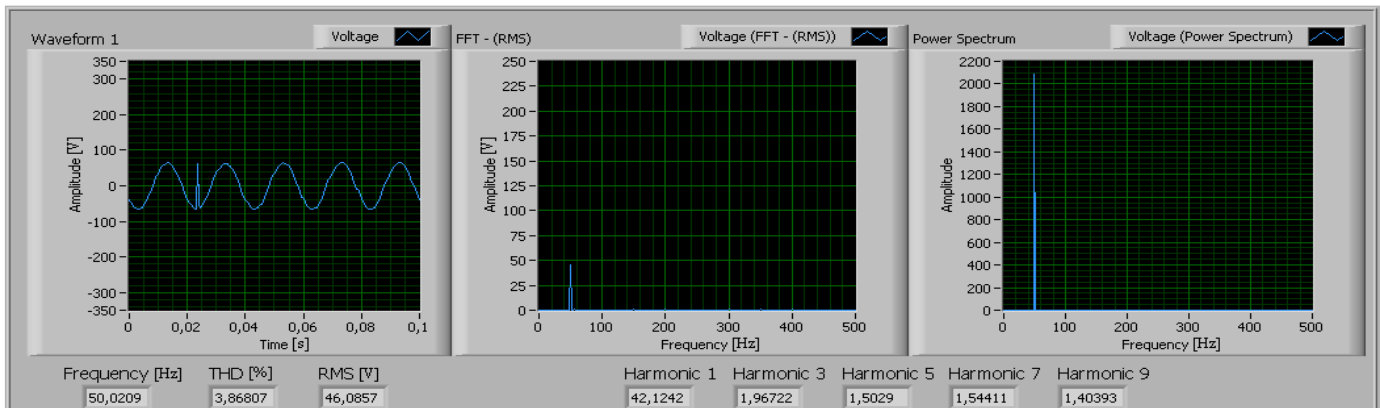
Fig. 8. High transient pulse caused by lightning
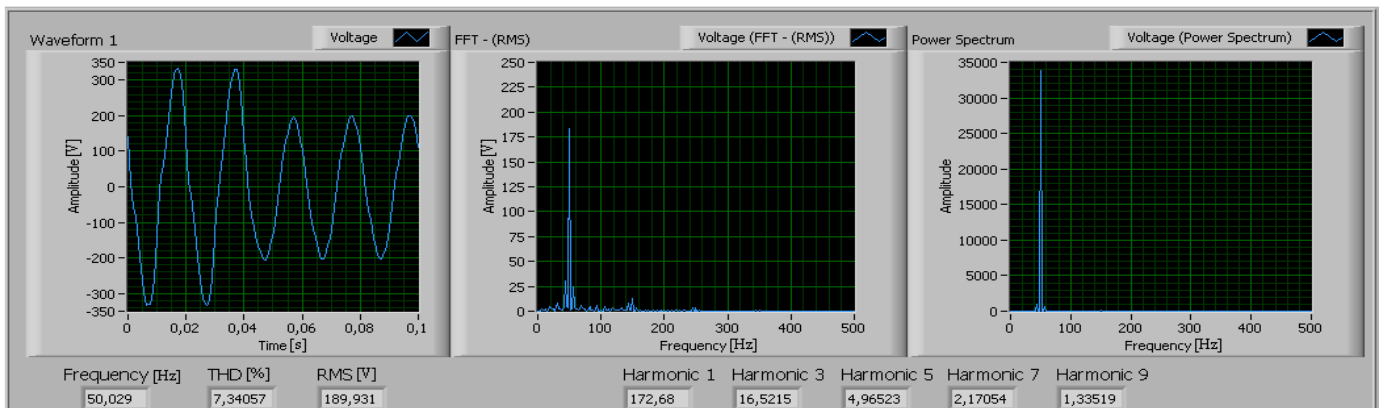
Fig. 9. Flicker with square distribution
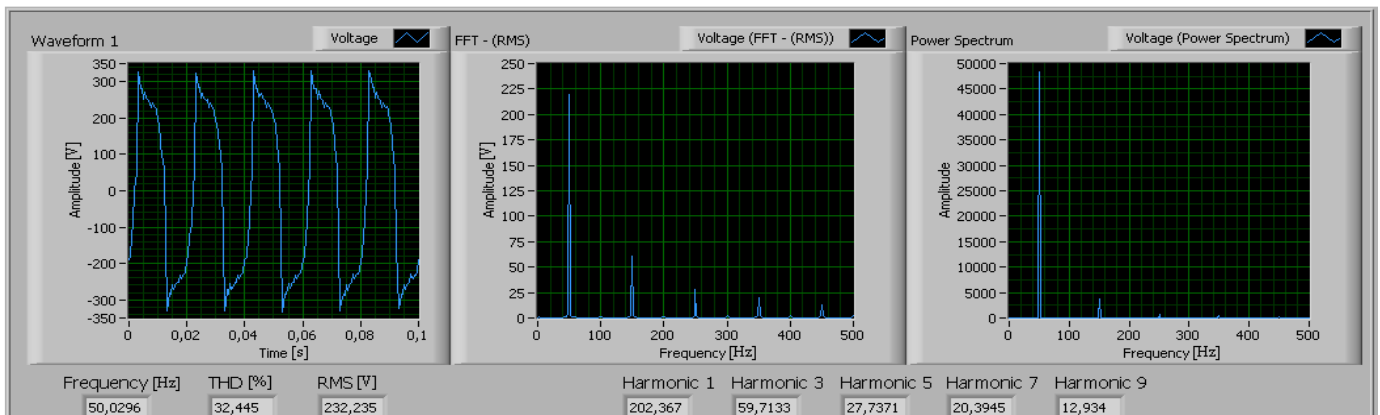
Fig. 10. Highly distorted signal of a simple chopper voltage converter
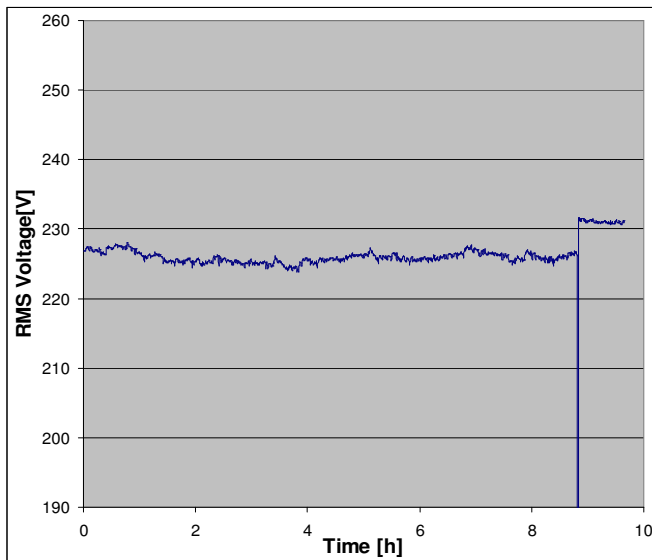
Fig. 11.a Current and power measurements block diagram
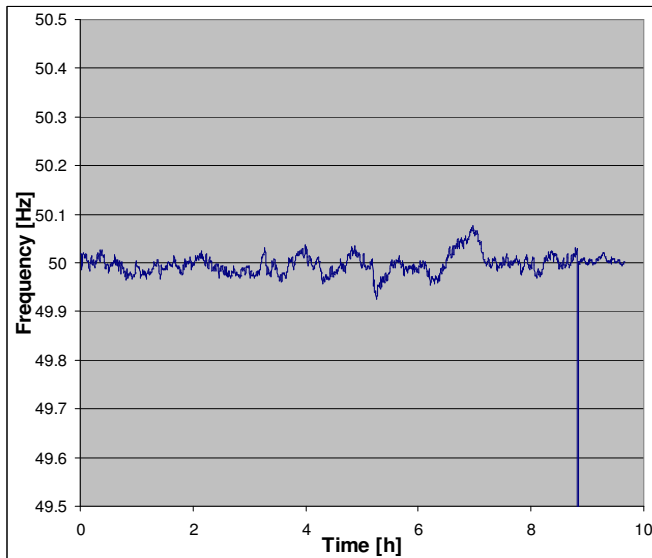
Fig. 11.b. Current and power measurements block diagram
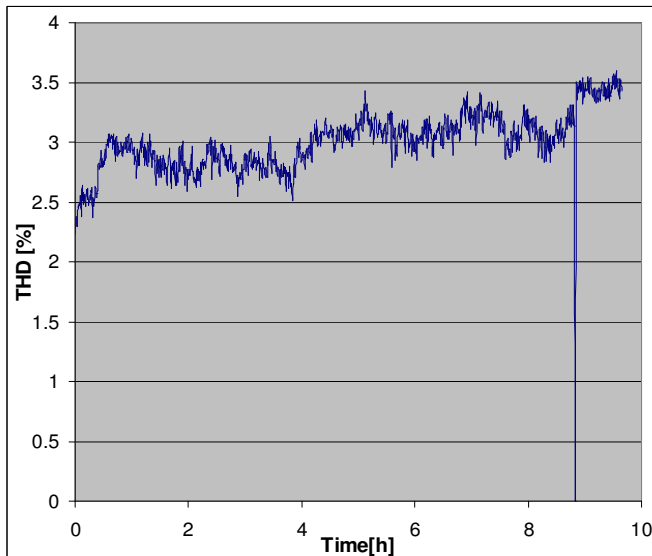
Fig. 11.c. Current and power measurements block diagram

In Fig.11.a, Fig.11.b and Fig.11.c recorded values for the RMS voltage, frequency and THD during 10 hour interval are presented. The graphs are obtained by using the data records from text files presented in MS Excel. The virtual instrument detected appearance of short voltage interruption, as it can be seen from the results.

VIII. CONCLUSIONS

This paper has summarizes theoretical and practical facts concerning the monitoring and analysis of power quality parameters. One possible hardware solution for signal conditioning in combination with DAQ card is implemented. This system is used for measurement and analyzes of different power quality disturbances. The signal conditioning module is developed in a way so it can be used for measurement of all power quality parameters. The voltage, current and power analyses are completely developed using virtual instrumentation techniques implemented in LabView software. Measurement data are recorded in text files for further analysis by using some graphical presentation software such as DIAdem or MS Excel. The performance of the proposed equipment is good enough for an effective application to test the power quality parameters.

The implemented system worked correctly in real time and detected and stored different types of disturbances.

REFERENCES

[1] M. H. J. Bollen, "What is power quality?", *Elect. Power Syst. Res.*, vol.66, pp. 5-14, 2003
[2] E. Acha, M. Madrigal. (2002, January) Power systems harmonics, Wiley
[3] R. G. Ellis, "Harmonic analysis of industrial power systems", *IEEE Trans. Ind. Apl.*, vol.32, no.2, pp.209-214, May 2001
[4] EN50160 Power quality standard, Power quality access meters and EN50160, Simens, May 2003
[5] G. Proakis, Dimitris G. Manolakis. (2007) Digital Signal Processing, Pearson Prentice Hall
[6] National Instruments, *LabView Measurements Manual*
[7] L. Cristaldi, A. Ferrero, R. Ottoboni: "Measuring   equipment for the Electric Quantities at the Terminals of an Inverter-Fed Induction Motor", IEEE Tech. Update Series, Instr. and Meas. Technology and Applications, ed. E. Petriu, 1998
[8] Power Simulator MI 2191 *Instruction Manual*
[9] D. Kottick. (2008, August) Power Quality monitoring system – voltage dips, short interruptions and flicker, *Elect. Power Qual. & Utilisagion Magazine* Vol.3. (Issue.2), [Online]. Available: http://www.scribd.com/doc/3306358/Power-Quality-Monitoring-System-Voltage-Dips-Short-Interruptions-and-Flicker
[10] A. Greenwood. (1991, April 4). Electrical transients in power systems (2nd ed.) [Online] . Available: http://www.amazon.ca/gp/reader/0471620580/ref=sib_dp_pt/187-5038544-5391220#reader-link

A Thyristor Full-Wave Rectifier With Full Control of the Conducting Angle

Ružica Stevanović

Abstract—**A new rectifier will be described capable of control of the conducting angle in the full range from zero to π. A two cell ledder RC network is studied first to enable design of a phase shifter. Then a halve-wave rectifier is described performing full control of the conducting angle. It incorporates a phase shifter implemented in the gate circuit of the thyristor. Using this a full wave rectifier is described and its characteristics extracted by simulation. The main andvantage of the new circuit is its ability to control the conducting angle in its full range making the rectifier applicable in both electronic power supply circuits and in systems that need power control.**

Index Terms—**AC/DC converter, power supply, full-wave thyristor rectifier.**

I. INTRODUCTION

THE need for control of the conducting angle in rectifiers comes from its applications related to power control. Both, in applications where electronic circuit power supply is planned and in industrial applications, one prefers having a circuit with such capabilities. Frequently one would need a rectifier with a full scale of control of the conducting angle from 0 to π. We will describe here a new circuit that has these characteristics. The fundamental idea implemented is to use a two cell RC ladder network as a phase shifter controlling the firing of the thyristor's gate.

The paper is organized as follows.

II. FULL-WAVE RECTIFYING BY A THYRISTOR

In Fig. 1 a general schematic of a full-wave controlled rectifier with thyristor is shown. The main voltage *E,* is rectified so that the thyristors are triggered by a control circuit which is, in this case, passive and consists of an RC ladder followed by a diac. The controll circuitry is not shown for convenience.

Fig. 2 represent the waveforms of the main voltage and the load voltage being denoted by V_{out}. As can be seen the conducting angle Θ_c may be less than π/2 but generally may be controlled between 0 and π. During the phase angle Θ_p, the thyristor is off.

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The controlling voltage for the thyristor's gate in our solution is derived from the main voltage, attenuated, phase shifted , and, finally, brought to the thyristors gate via diac performing as a threshold element and protecting from conducting in the inverse direction. This is why we first address the phase shift circuit in the next.
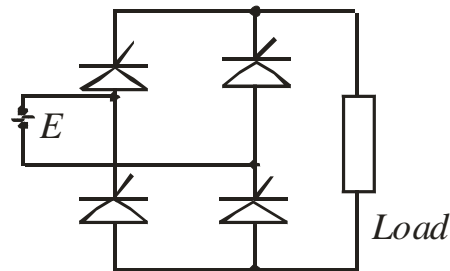
Fig. 1. Block scheme of Full-wave controlled rectifier.
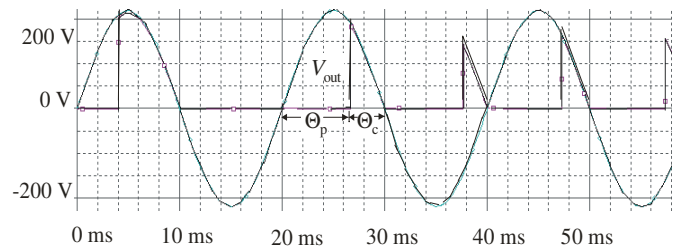
Fig. 2. Flowing angle.

III. RC CIRCUIT AS ELEMENT OF COMPLEX CIRCUIT

The single cell passive RC circuit is known to produce a maximum phase shift of π/2 in asimptotic conditions i.e. for infinite frequency. Having in mind that our frequency is fixed to 50 Hz very large values of the RC elements are needed even for angles neer to π/2. Having that in mind and intending to extend the possibilities of the controlling circuit we in [3] proposed the use of two-cell passive RC ladder circuit as depicted in Fug. 3. Its frequency domain characteristics were studied in [1].

The voltage transfer function of this circuit is given with [1]

$$T(s) = \frac{V_{out}}{E} = \frac{1}{1 + s(\tau_1 + k\tau_2) + s^2 \tau_1 \tau_2} \qquad (1)$$

where is $\tau_1 = R_1 C_1$, $\tau_2 = R_2 C_2$, and $k = R_1/R_2$. In the case $R_1 = R_2 = R$ and $C_1 = C_2 = C$ the poles of function (1) are $s_1 = s_2 = -1/\tau$, where is $\tau = RC$.

The phase characteristic of this function for the case when $R_1 = R_2 = R$ and $C_1 = C_2 = C$ is given by

$$\varphi = \mathbf{Arg}[T(s)]\big|_{s=j\omega} = -2 \cdot \mathbf{arctg}(\omega RC) \qquad (2)$$
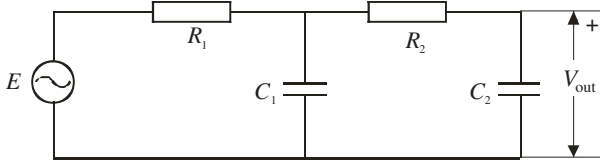
Fig. 3. Circuit of two RC sections.

As the signal frequency is fixed, the dependence of phase angle on resistance and capacitance is of interst. $\varphi = f(R,C)$ is obtained using the programme SPICE [4]. The simulation results are shown in Fig. 4.
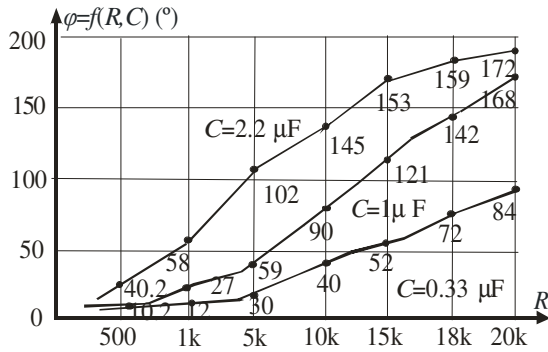
Fig. 4. Phase angle circuit with two RC sections.

Fig. 4 represents the phase angle dependence on the resistance in the RC ledder for three different values of the capacitance. By inspection of the results one may conclude first that resistances no larger than 20 kΩ are needed for the application conceived. As for the capacitances we may come out with the conclusion that $C=1\mu$F is practicaly satisfactory and, in fact, the most convenient value. Having in mind these consideration we came to the conclusion that one needs to fix the capacitance value and to use variable resistances for control of the phase angle. Note that resistors with variable resistance are easier to implement or to get from the market.

The amplitude characteristic of the function (1) in the case when $R_1 = R_2 = R$ and $C_1 = C_2 = C$ is obtained as

$$A = \big|T(s)\big|\big|_{s=j\omega} = 1/\sqrt{[1+(\omega RC)^2]^2} = 1/[1+(\omega RC)^2] \qquad (3)$$

or, in terms of decibells,

$$a\,(\mathrm{dB}) = 20 \cdot \mathbf{log}(1/A) = f(R,C). \qquad (4)$$

As for the phase characteristic, using SPICE we got the dependence a=f(RC) so that we fixed the value of the capacitance and put the resistance in the role of a variable. The results are depicted in Fig. 5.

From the amplitude characteristics depicted in Fig. 5 we may come to the conclusion that even for the largest values of the resitances, if C = 1 μF, we get an attenuation of only about
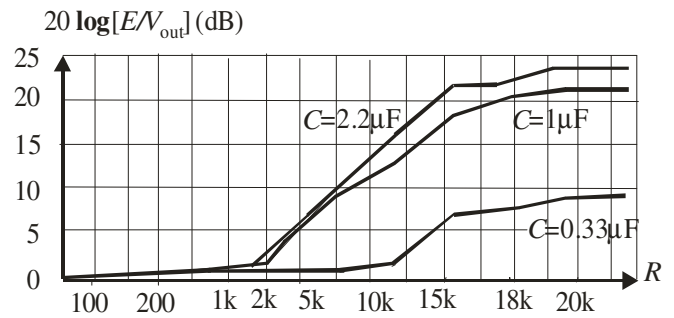
Fig. 5. Attenuation of circuit with two RC sections.

20 dB that is about ten times. This means that one may expect voltages of the order of magnitude no less than 25 V at the otput of this circuit. This considerations are important for the choice of the diac that usually follows the RC ledder.

From the designers point of view, given the phase angle and the value of the capacitance C = 1 μF, for value of the resistance, one may use

$$R = \frac{2}{\omega C} \cdot \left[\mathbf{tg}\left(\left|\theta_p\right|/2\right)\right] \qquad (5)$$

what is derived from (2). This derivation are fully approved by inspection of Fig. 4 as discussed in [3].

IV. HALF-WAVE THYRISTOR RECTIFIERS WITH CONDUCTION ANGLE CONTROL

The first implementation of the two-cell RC ledder in a thyristor rectifier is depicted in Fig. 6 [3]. The thyristor is triggered by the gate current pulses that are emanated from main voltage and shaped by the control circuit. The main task of the diac to generate a voltage threshold which, whem is overshoted, leads the gate to conducting state. In the negative half cycle of the main voltage the DIAC and the thyristor are off.
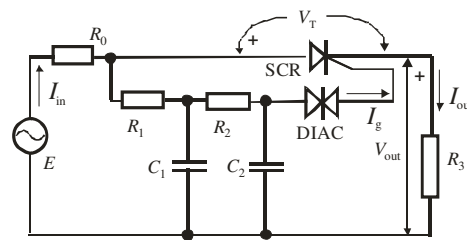
Fig. 6. Half-wave rectifier using a two-cell RC ledder.

Fig. 7. shows the transient waveform of the output voltage just after switching on the circuitry. As can be seen the phase angle is in accordance with the value that, for the given circuit parameters, may be extracted from Fig. 4. Fig. 8. depicts the current waveforms i.e. the load current (I_{out}), the main current (I_{in}) and thyristor's gate current (I_g).

Finally, Fig. 9. depicts voltage waveforms for the case when $R=20$ kΩ. One may notice that conducting angles are considerably lower than 90°.

After exhaustive simulations, Fourier analisys of the waveforms obtained for large set of values of the resistance in the phase delay circuit, the spectra of the voltages are
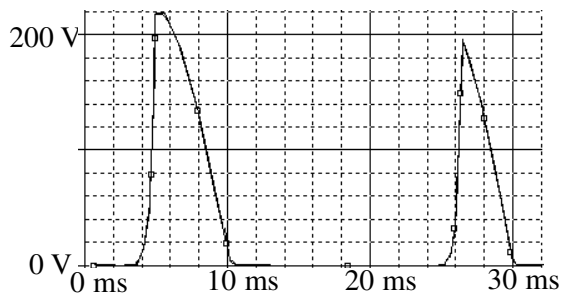
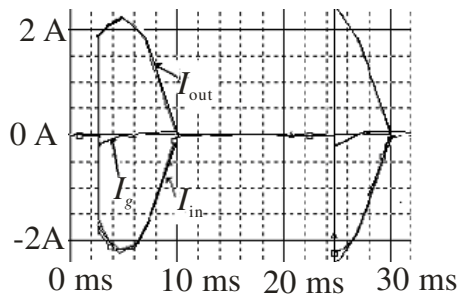Fig. 7. Waveforms of the output voltage of the circuit of Fig. 6 (for R=10kΩ, C=1μF, and R_3=100Ω).

Fig. 8. Waveforms of the currents in the circuit of Fig. 6 (for R=10kΩ, C=1μF, and R_3=100Ω).
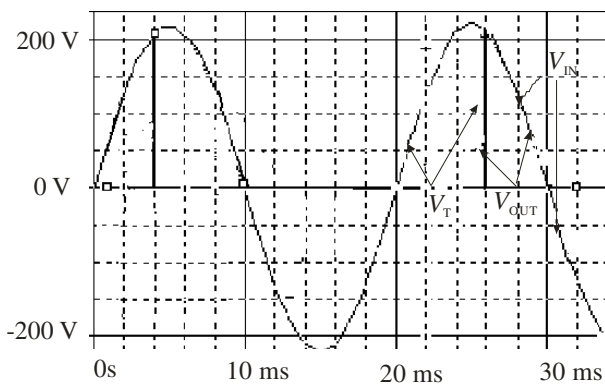

Fig. 9. Voltage waveforms (for R=20kΩ, C=1μF, and R_3=100Ω).

obtained. Part of these results are shown in Fig. 10 where the DC component of the output voltage is depicted as a function of the resistance in the phase delay circuit, for two values of the load resistance.
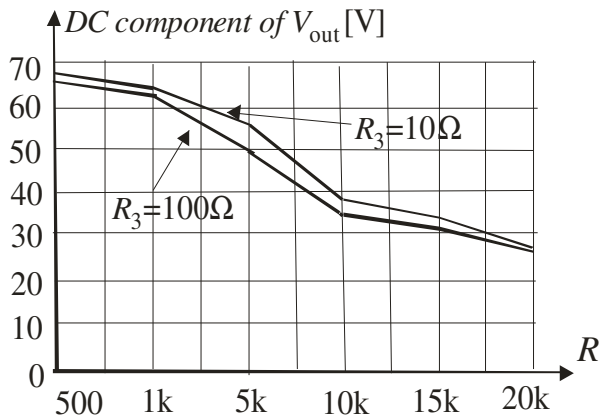

Fig. 10. Direct component of load voltage the Half-wave rectifier.

The magnitude of the first harmonic of the output voltage as a function of the resistance in the phase delay circuit for two

values of the load resitance is depicted Fig.11. As cen be seen by comparing the results of Fig. 10 and Fig. 11, the alternating component of the voltage is dominant for all values of the resistance in the phase delay circuit. Nevertheles, this dominance is less persuasive for large values of resistance in the phase delay circuit.
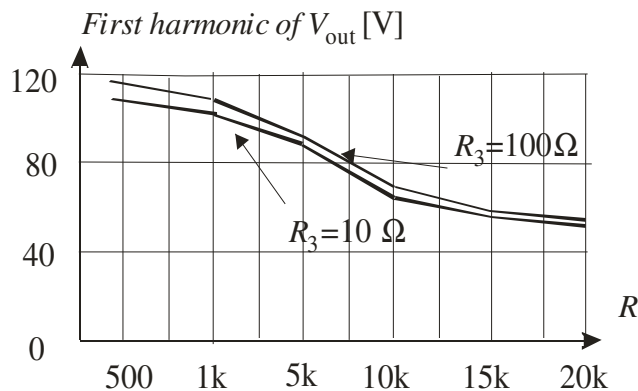
Fig. 11. The first harmonic of voltage on consumer in Half-wave rectifying.

V. FULL-WAVE CONTROLLED RECTIFIER WITH CONTROL ANGLE OF PHASE

In order to get larger DC component in the full spectra of the obrained signal at the output full-wave rectification is needed. Application of the circuit of Fig. 6. in a full-wave rectifyer is depicted in Fig. 12 and Fig. 13. Note that for simplification of the schematic we introduced a subcircuit denoted by D as shown in Fig. 12a. Fig. 12b represents a version of the full-wave rectifier in which a transformer is implemented while Fig. 13 represents a transformeless version of the rectifier. The advantages and disadvantages of these two solutions are known to the scientific public and will be not discussed here.

The full wave rectifier circuit was simulated by the SPICE program in the same manner as the half-wave circuit. The resulting simulation results are shown in the next.

In Fig. 14 the output voltage waveforms are depicted. One can notice that after transient a steady response is obtained in this case with conducting angle lower than $\pi/2$. In the same time one can recognize that the firing moment is in accordance with the phase angle obtained from Fig. 4.

The waveform of the output current is depicted in Fig. 15.

In the next influence of variations of the resistance in the phase shift circuit will be studied. In that sense R=5 kΩ was chosen firs. The simulation results for the output voltage are depicted in Fig. 16. Relativly large conducting angle may be observed.

Finally, a large value for teh resistance in the phase shift circuit was chosen: R=19 kΩ. The simulation results for the output voltage are shown in Fig. 17, while Fig. 18 represents the waveform of the output current. One may notice that after some transient a response is obtaine with very short pulses confirming the role of the controlling circuit.
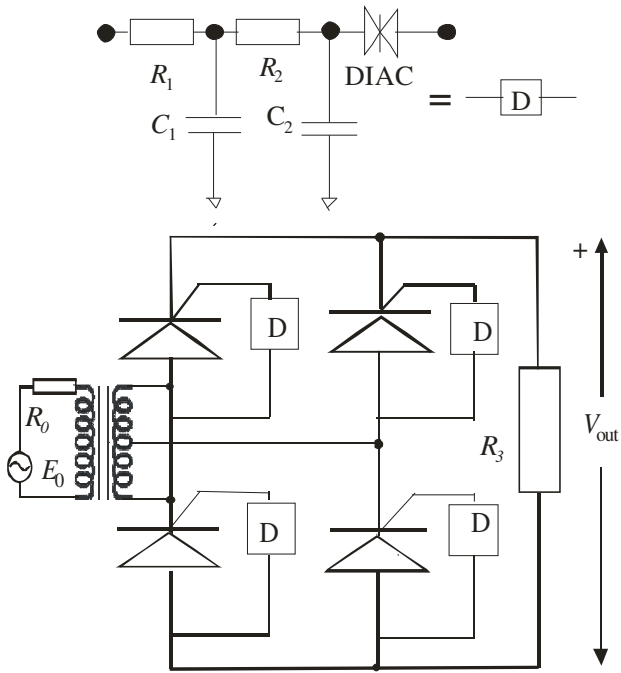
Fig. 12. (a) Symbol from the filter plus diac circuit, and (b) Full-wave controlled rectifier with transformer.
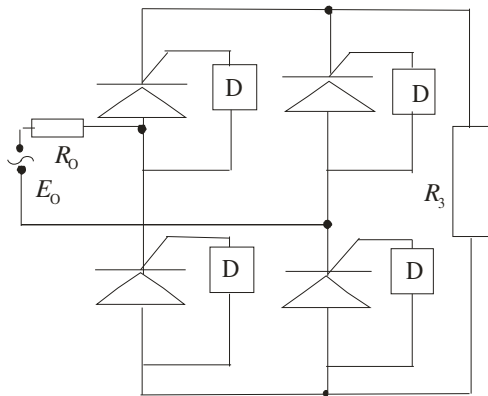

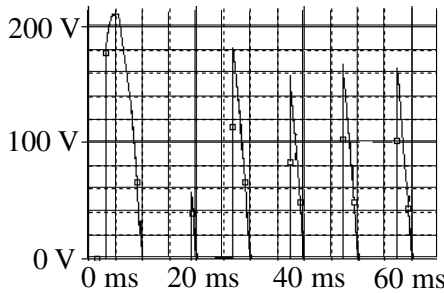Fig. 13. Block scheme circuit for Full-wave controlled rectifier without transformer.

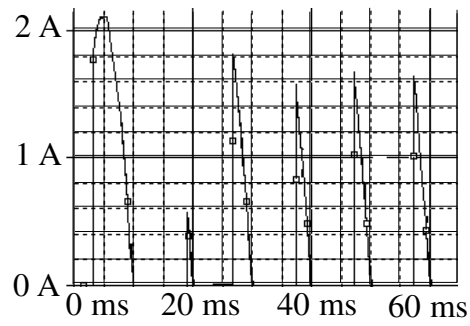Fig. 14. Waveform of output voltage (for $R=12k\Omega$, $C=1\mu F$, and $R_3=100\Omega$).

Fig. 15. Waveform of output current (for $R=12k\Omega$, $C=1\mu F$, and $R_3=100\Omega$).
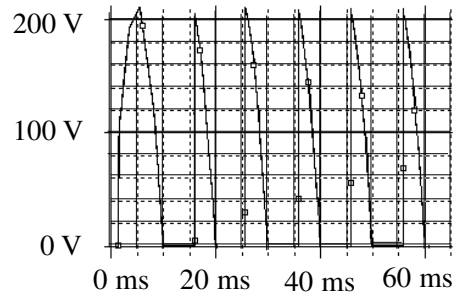
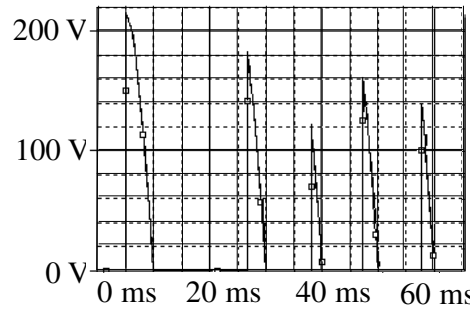Fig. 16. Waveform of voltage (for $R=5k\Omega$, $C=1\mu F$, and $R_3=100\Omega$).

Fig. 17. Output voltage waveform (for $R=19k\Omega$, $C=1\mu F$, and $R_3=100\Omega$).
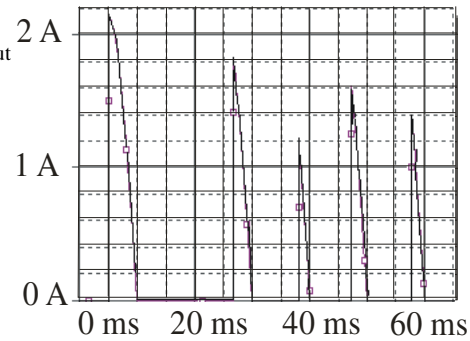
Fig. 18. Output current waveform (for $R=19k\Omega$, $C=1\mu F$, and $R_3=100\Omega$).

To get a full picture of the properties of the new proposed circuit Fourier analysis of the output voltage waveforma was performed for a set of resistances R and for two values of the load resistance i.e. $R_3=10\Omega$ and $R_3=100\Omega$.

The results obtained after Fourier analysis are depicted in Fig. 19 and Fig. 20. The first one represents the DC component of the output voltage as a function of the resistance in the phase shift circuit. One may notice a floor of about 50V that is not dependent on the load resistance. On the other side, Fig. 20 depicts the dependence of the second harmonic on the resistance in the phase shift circuit. Again, as expected, for small conducting angles large harmonic compared with the DC value is obtained. Note, however, that that is the second harmonic meaning that in use of such rectifier for electronic power supply circuit easier filtering is enabled.
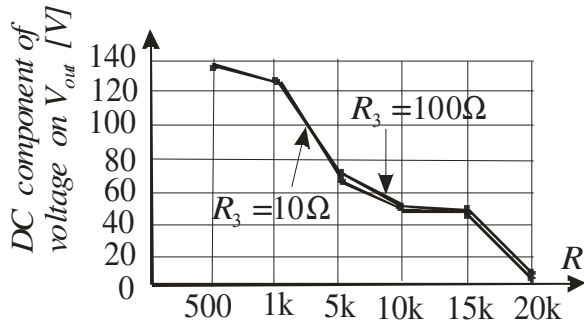
Fig. 19. DC component of output voltage of the Full-wave rectifier.

Fig. 20. The second harmonic of voltage on load.

VI. CONCLUSION

A new concept of control of the conducting angle of a thyristor rectifier was proposed and implemented in hal-wave and full-wave rectification circuits. After theoretical study of the circuit and after creation of some design formulae a thorough verification procedure was implemented based on SPICE simulation of the circuits. In particular, the properties of the circuits in the frequency domain were studied in order to produce information of the aplicability of the circuit in different applications.

It is our oppinion that the concept proposed is promising and we expect in the future to get further improvement by introducing voltage controlled resistors so enabling phase angle control by single controlling signal.

REFERENCES

[1] Litovski, V. „*Basics of Electronics*", Akademska misao, Belgrade, 2006, in serbian.

[2] Dokić, B. „*Power electronics –converters and regulators*", ETF Banja Luka, 2000, in serbian.

[3] Stevanović, R. „Thyristor rectification with conducting angles less than 90 degrees", Tehnika, Belgrade, No. 4, 2008, accepted for publication, in serbian.

[4] Banzaf, W., „Computer-Aided Circuit analysis using SPICE", Prentice Hall, Enlewood Cliffs, N. J., 1989.

[5] Taylor,P.D., „Thyristor design and realization", John wiley and Sons, Chichester, 1987.

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ELECTRONICS, VOL. 13, NO. 1, JUNE 2009